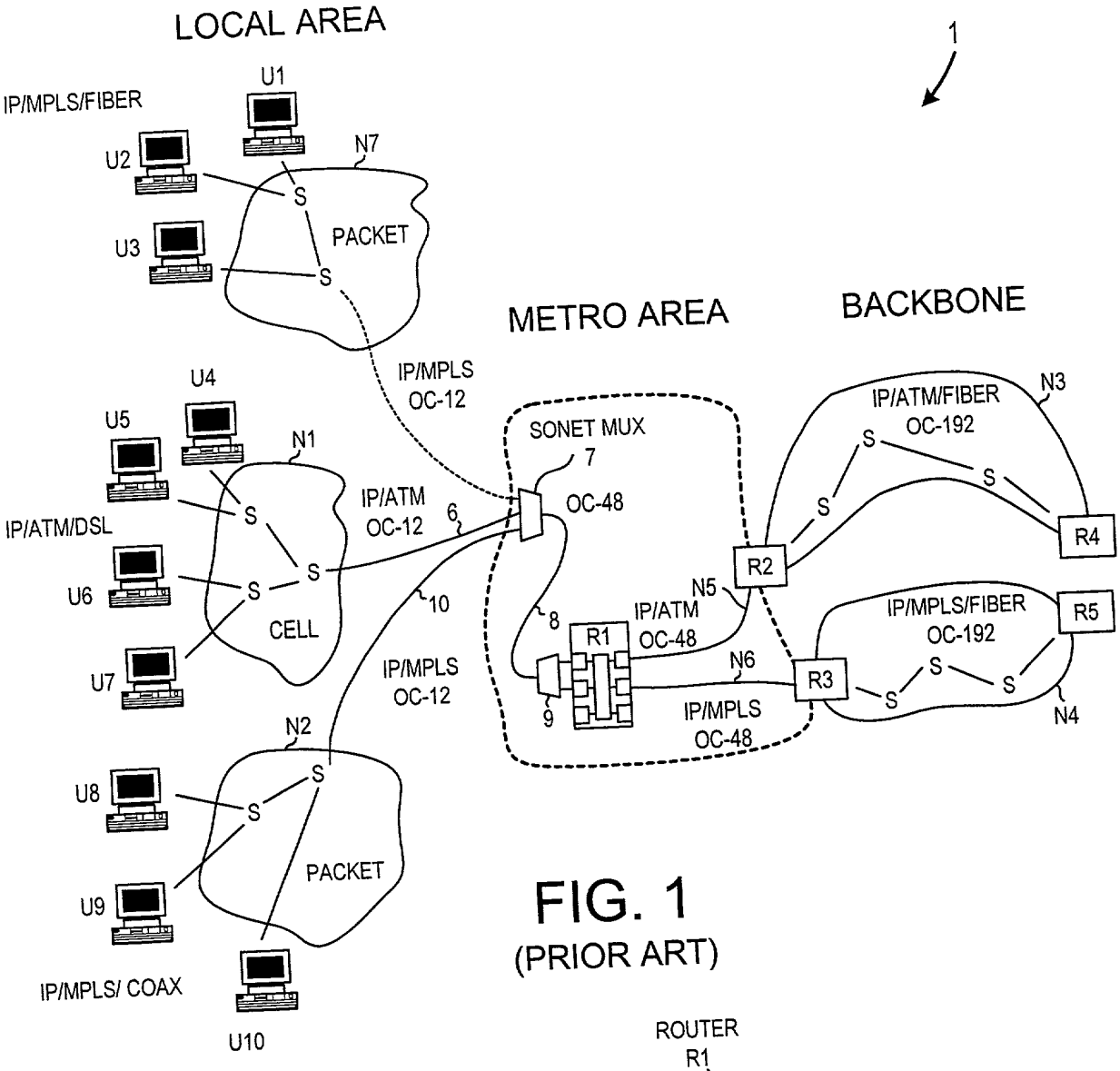


FIG. 1
(PRIOR ART)

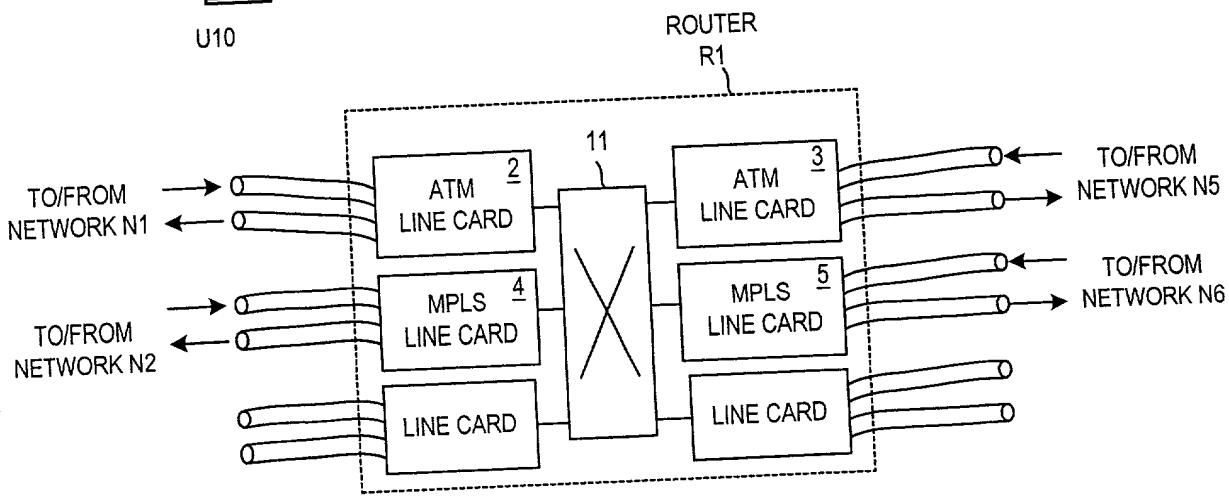


FIG. 2
(PRIOR ART)

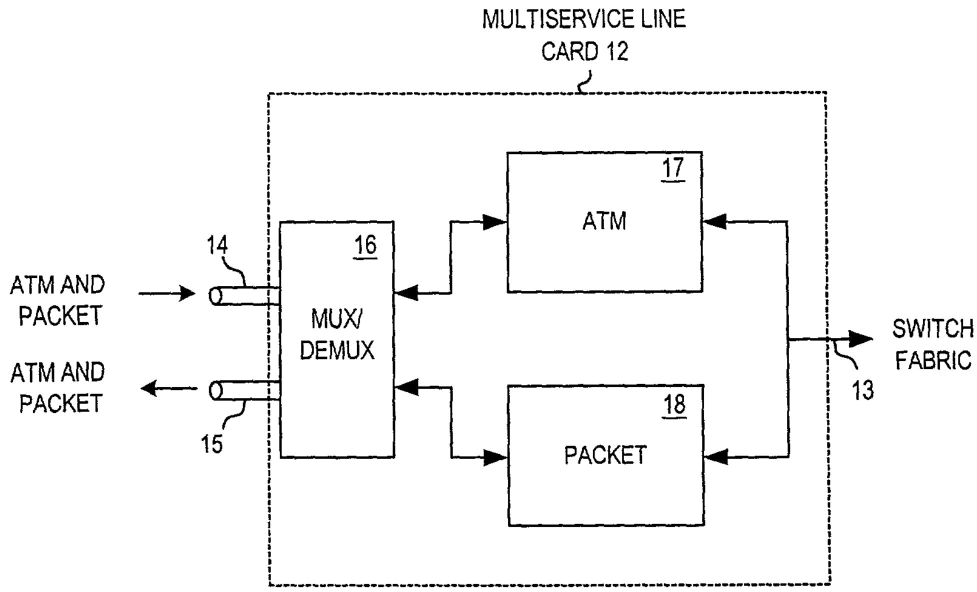

MULTISERVICE LINE
CARD 12
17
ATM
16
14
ATM AND
PACKET
MUX/
DEMUX
SWITCH
FABRIC
ATM AND
PACKET
13
18
PACKET
15

FIG. 3

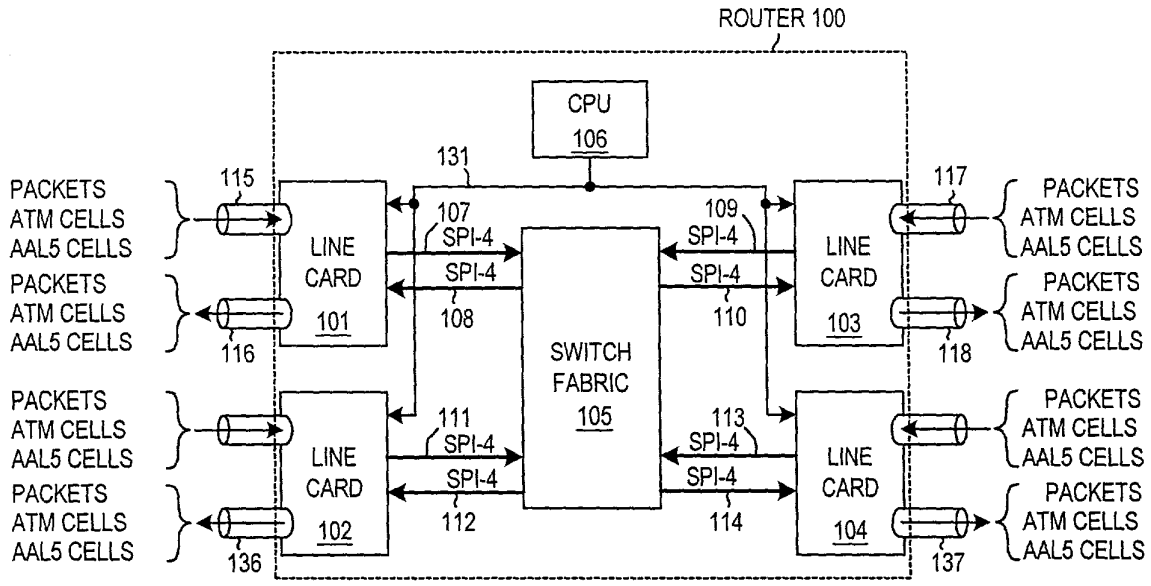

ROUTER 100
CPU
106
131
PACKETS
ATM CELLS
AAL5 CELLS
115
116
117
118
LINE
CARD
101
LINE
CARD
103
LINE
CARD
102
LINE
CARD
104
SWITCH
FABRIC
105
107
SPI-4
108
109
SPI-4
110
111
SPI-4
112
113
SPI-4
114
136
137

FIG. 4

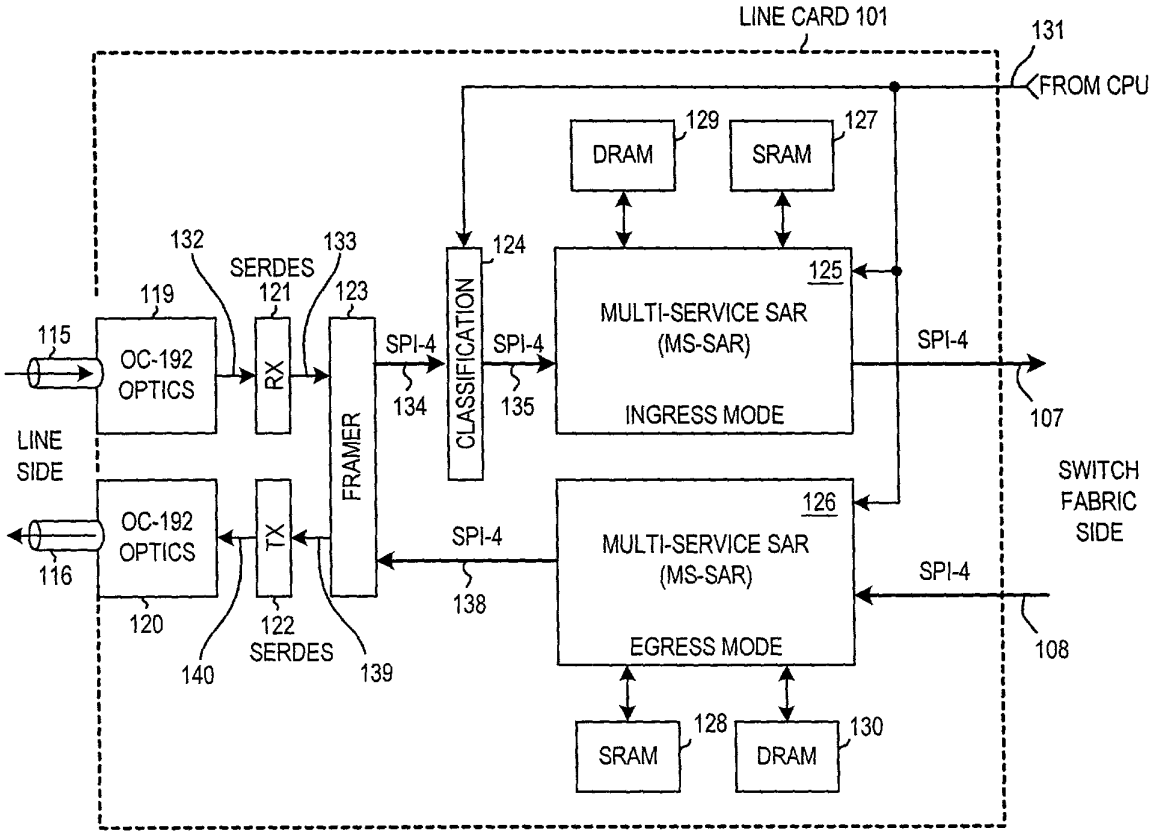

LINE CARD 101
131
FROM CPU
DRAM
129
SRAM
127
125
MULTI-SERVICE SAR
(MS-SAR)
INGRESS MODE
124
CLASSIFICATION
132
SERDES
121
133
123
119
115
OC-192
OPTICS
RX
FRAMER
SPI-4
134
SPI-4
135
SPI-4
107
LINE
SIDE
SWITCH
FABRIC
SIDE
126
MULTI-SERVICE SAR
(MS-SAR)
EGRESS MODE
SPI-4
138
SPI-4
108
116
OC-192
OPTICS
TX
120
122
SERDES
140
139
SRAM
128
DRAM
130

FIG. 5

SWITCH FABRIC	APPLICATION TYPE	INGRESS APPL TYPE	EGRESS APPL TYPE
CELL	ATM => ATM	0	8
	ATM => MPLS PACKET	1	9
	MPLS PACKET => ATM	2	10
	MPLS PACKET => MPLS PACKET	3	11
PACKET	ATM => PACKET	4	14
	PACKET => ATM	6	12
	AAL5 => PACKET	5	14
	PACKET => AAL5	6	13
	PACKET => PACKET	6	14

APPLICATION TYPES

FIG. 6

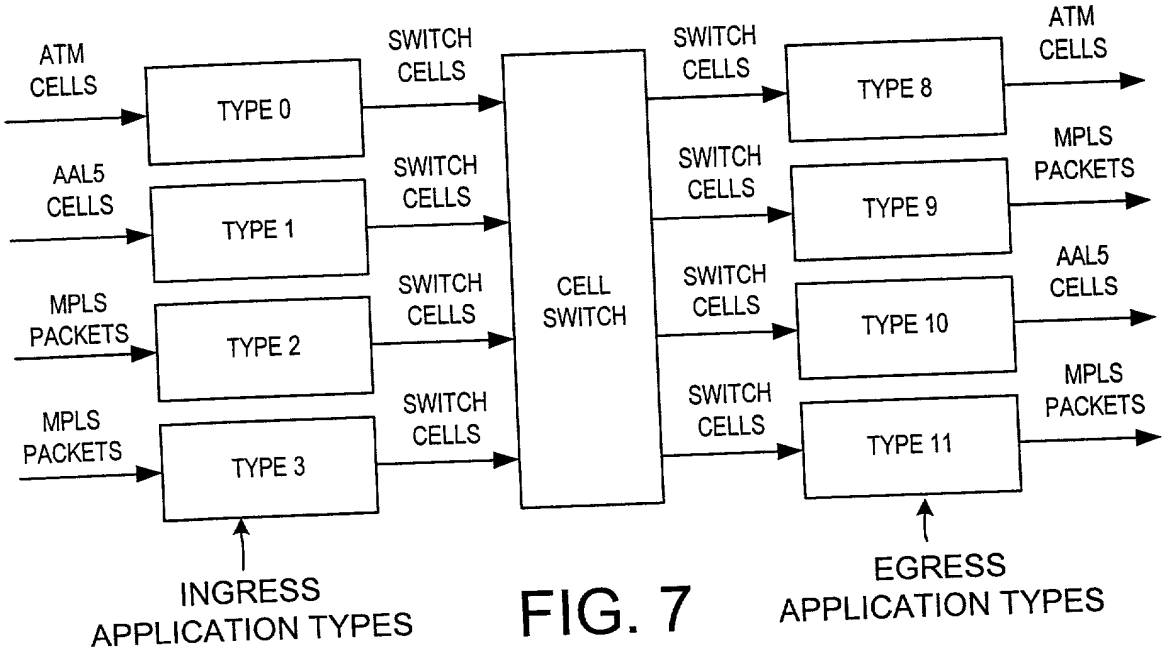


FIG. 7

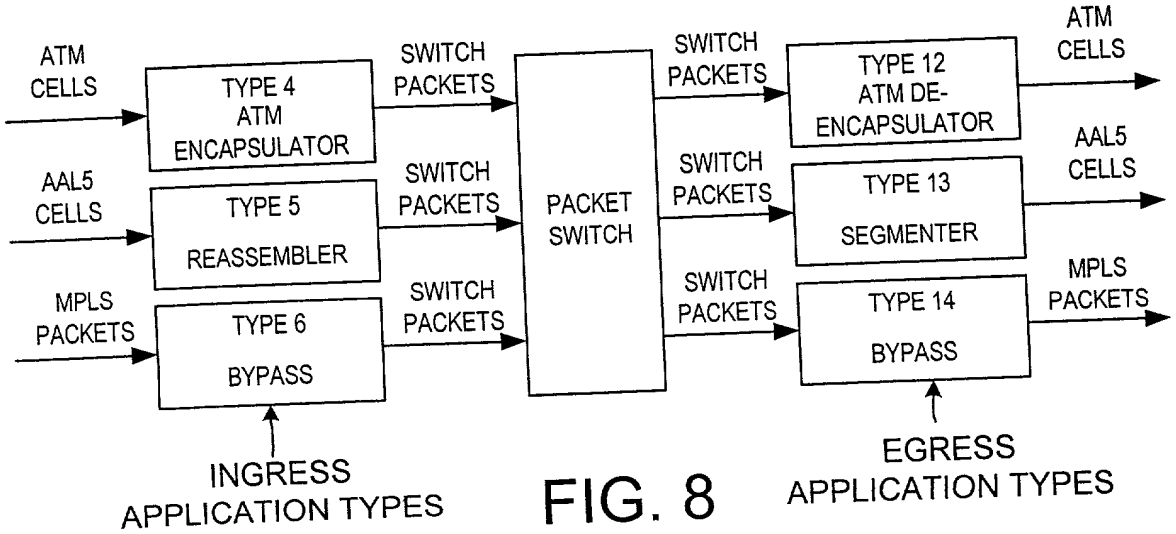


FIG. 8

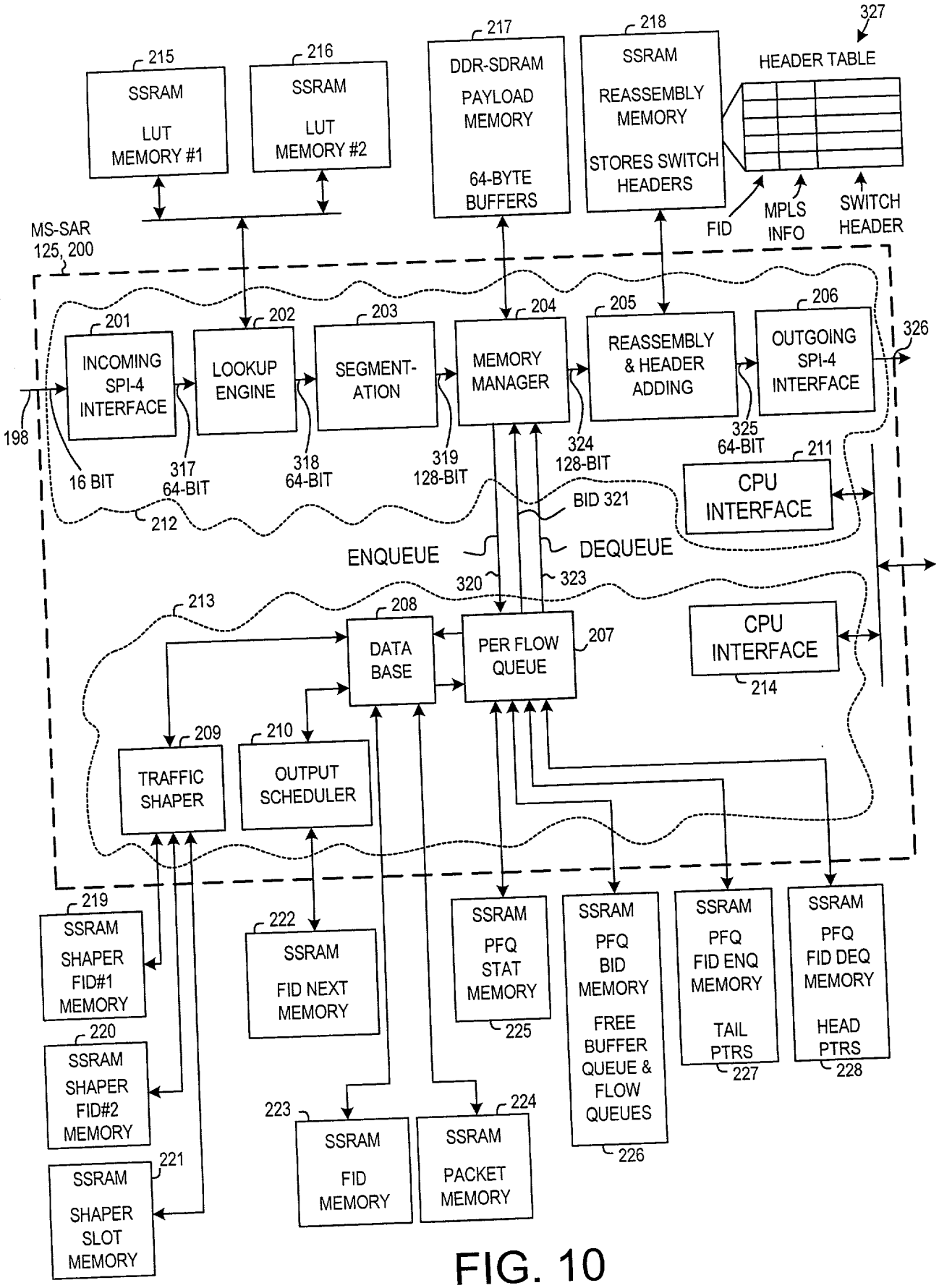

215
SSRAM
LUT
MEMORY #1
216
SSRAM
LUT
MEMORY #2
217
DDR-SDRAM
PAYLOAD
MEMORY
64-BYTE
BUFFERS
218
SSRAM
REASSEMBLY
MEMORY
STORES SWITCH
HEADERS
327
HEADER TABLE
FID
MPLS
INFO
SWITCH
HEADER
MS-SAR
125, 200
201
INCOMING
SPI-4
INTERFACE
202
LOOKUP
ENGINE
203
SEGMENT-
ATION
204
MEMORY
MANAGER
205
REASSEMBLY
& HEADER
ADDING
206
OUTGOING
SPI-4
INTERFACE
326
198
16 BIT
317
64-BIT
318
64-BIT
319
128-BIT
324
128-BIT
325
64-BIT
211
CPU
INTERFACE
212
BID 321
ENQUEUE
DEQUEUE
320
323
213
208
DATA
BASE
PER FLOW
QUEUE
207
CPU
INTERFACE
214
209
TRAFFIC
SHAPER
210
OUTPUT
SCHEDULER
219
SSRAM
SHAPER
FID#1
MEMORY
222
SSRAM
FID NEXT
MEMORY
SSRAM
PFQ
STAT
MEMORY
225
SSRAM
PFQ
BID
MEMORY
FREE
BUFFER
QUEUE &
FLOW
QUEUES
226
SSRAM
PFQ
FID ENQ
MEMORY
TAIL
PTRS
227
SSRAM
PFQ
FID DEQ
MEMORY
HEAD
PTRS
228
220
SSRAM
SHAPER
FID#2
MEMORY
221
SSRAM
SHAPER
SLOT
MEMORY
223
SSRAM
FID
MEMORY
224
SSRAM
PACKET
MEMORY

FIG. 10

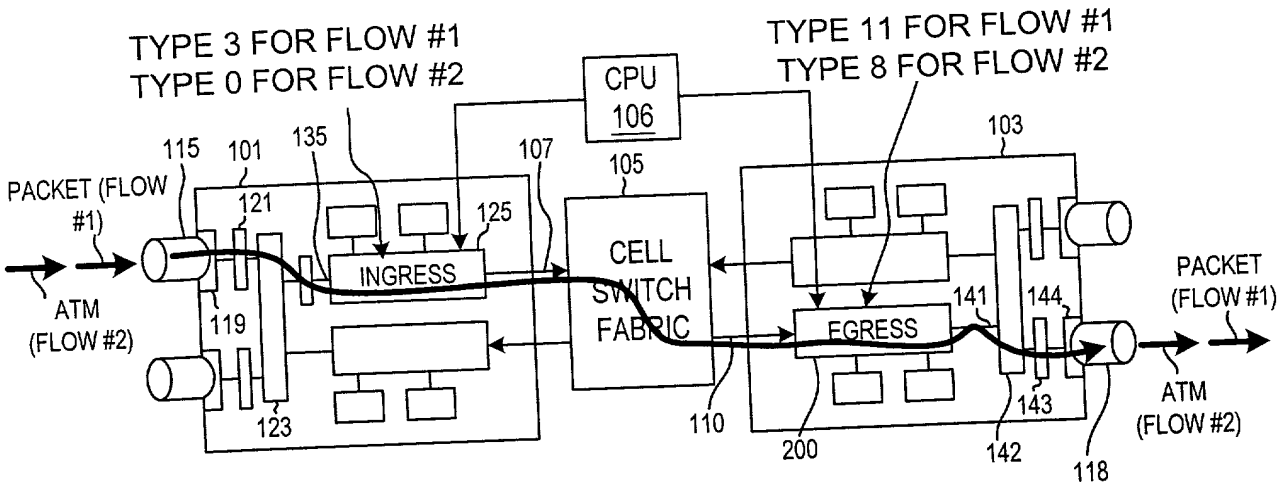


FIG. 9

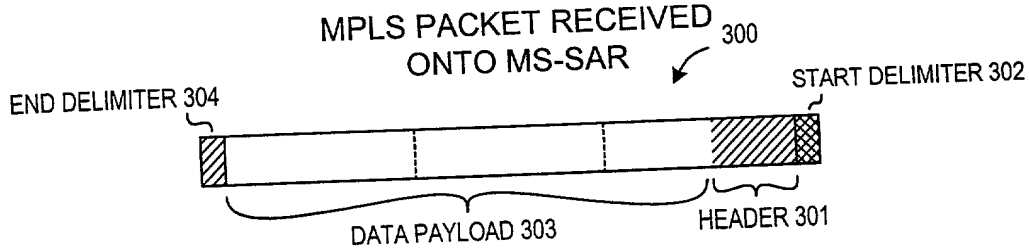


FIG. 11

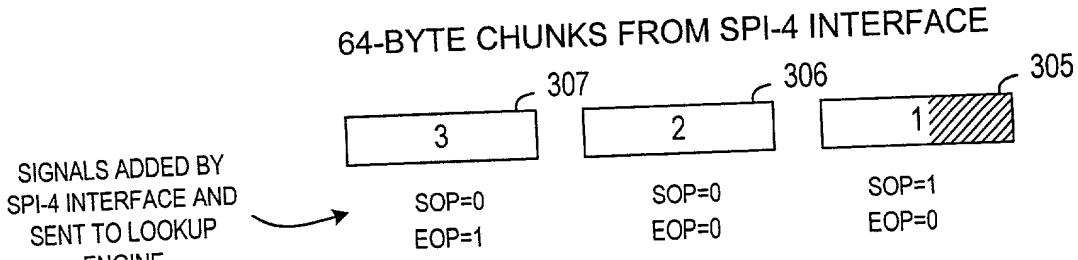
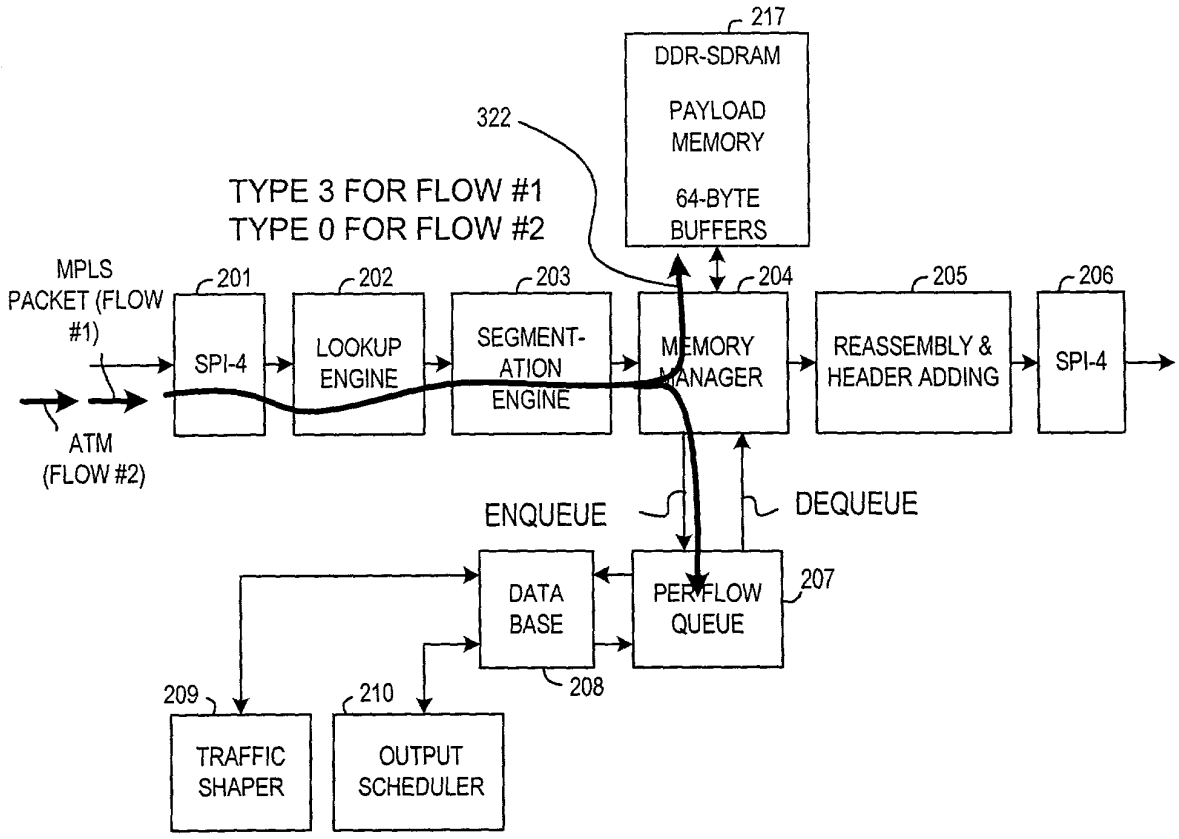


FIG. 12



INGRESS MODE

FIG. 13

PORT TABLE IN LOOKUP BLOCK

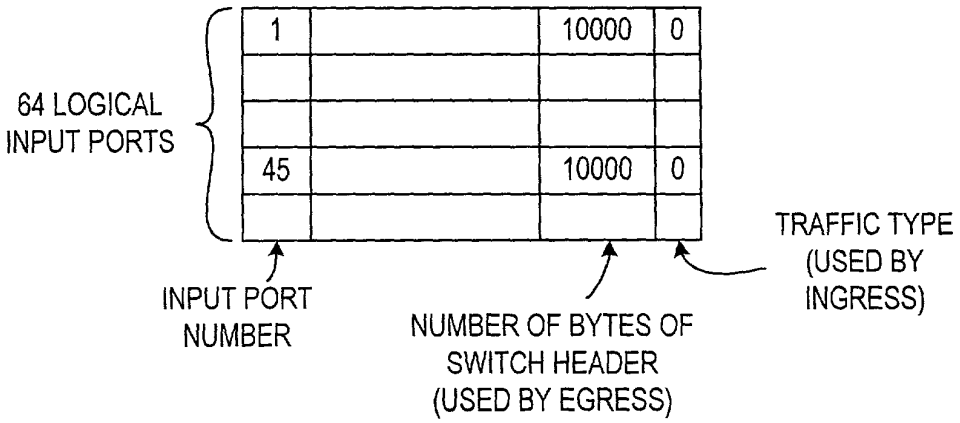


FIG. 14

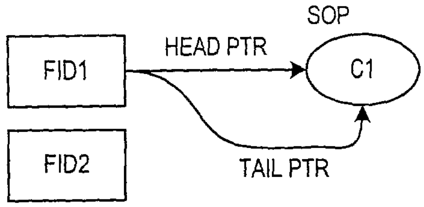


FIG. 15A

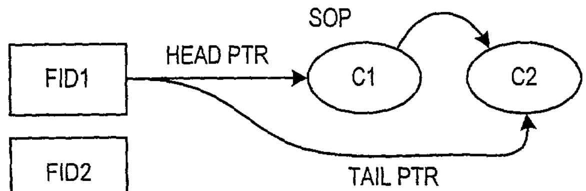


FIG. 15B

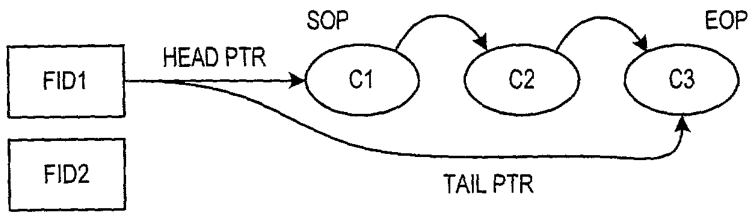


FIG. 15C

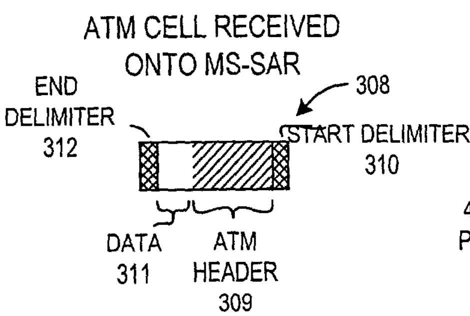


FIG. 20

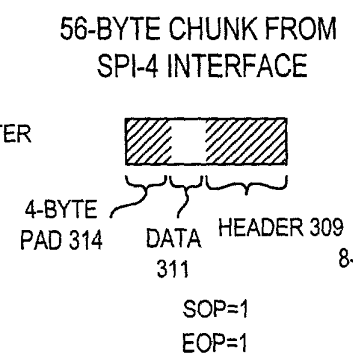


FIG. 21

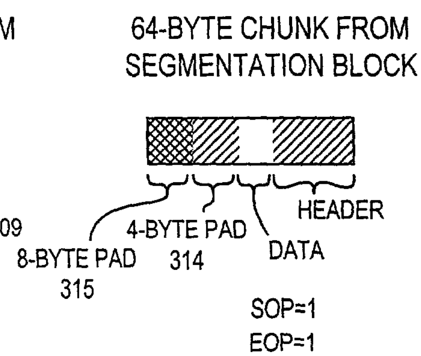


FIG. 22

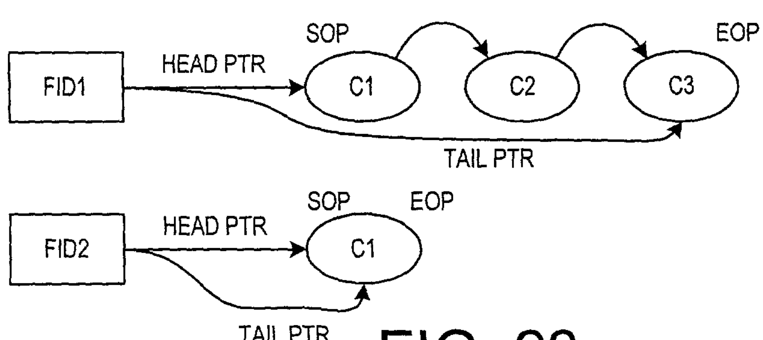


FIG. 23

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID HEAD	23	22:0	H	HEAD POINTER. FIRST BUFFER TO BE ENQUEUED, AND FIRST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
HD EOP PKT	1	23	H	IF SET, THE HEAD BID IS THE EOP.
HD SOP PKT	1	23	H	IF SET, THE HEAD BID IS THE SOP.
HD EFCI	1	25	H	EFCI BIT.
CLP	1	26	H	CLP BIT. CAN BE MODIFIED BY DBS.
OAM	1	27	H	OAM BIT.
SPARE	1	28	H	
CLASS	3	31:29	H	CLASS OF FID.
FID TYPE	4	35:32	H	APPLICATION TYPE INDICATES THE PROCESSING THAT THE MS-SAR WILL TAKE ON THIS FLOW. WILL BE SENT TO MEMORY MANAGER. TYPE IS WRITTEN WITH THE HEAD POINTER.

FID DEQUEUE MEMORY LOCATION

FIG. 16

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID TAIL	23	22:0	H	TAIL POINTER. LAST BUFFER TO BE ENQUEUED, AND LAST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
BID PRV PKT TAIL	23	45:23	H	BID OF PREVIOUS PACKET'S TAIL BID. SAVED ON EOP.
TTL	1	46	H	WHEN 1, DISCARD AND DEACTIVATE THE FID.
OUTPUT PORT#	7	53:47	S	OUTPUT PORT NUMBER THAT THE FID WILL BE TRANSMITTED ON.
Q SIZE	18	71:54	H	SIZE OF THE QUEUE IN BIDS. INCREMENTED ON ENQUEUE. DECREMENTED ON EVERY DEQUEUE OPERATION.

FIRST FID ENQUEUE MEMORY LOCATION

FIG. 17

NAME	NO BITS	RANGE	WR	DESCRIPTION
VALID	1	0	S	IF SET, THEN ENQUEUE. IF NOT, THEN SETUP CONNECTION COMMAND AS NEEDED BEFORE ENQUEUE STARTS.
SPARE	8	8:1		
DROP UNTIL SOP	1	9	H	DROP UNTIL THE NEXT SOP.
SEL DROP COUNT ER	1	10	H	SEL THE COUNT FOR DROPPING.
SPARE	2	12:11		
CURRENT TAIL PKT CELL CNT	11	23:13	H	REPRESENTS THE NUMBER OF CELLS IN THE TAIL PACKET THAT IS BEING ENQUEUED.
SPARE	2	25:24		
ENQ NOT DISCARD RED PKT COUNT	16	41:26	H	THE NUMBER OF NOT DISCARDED PACKETS THAT HAVE ARRIVED SINCE LAST RED DISCARD. IT IS RESET ON THE NEXT RED DISCARD.
SPARE	2	43:42		
AVG	18	61:44	H	THE AVE SIZE OF THE QUEUE.

SECOND FID ENQUEUE MEMORY LOCATION

FIG. 18

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID LINK	23	22:0	H	BID OF THE NEXT BUFFER IN FID QUEUE. ALSO CAN BE A BID LINKED ON THE FREE BUFFER QUEUE.
EOP PKT	1	23	H	END OF PACKET FOR THIS BID BID. EOP BELONGS TO THE BID LINK.
SOP PKT	1	24	H	START OF PACKET FOR THE CORRESPONDING BID. SOP BELONGS TO THE BID LINK.
EFCI	1	25	H	EFCI PASS THROUGH BIT.
OAM	1	26	H	OAM BIT.
CLP	1	27	H	CLP
SPARE	8	35:28		

BID MEMORY LOCATION

FIG. 19

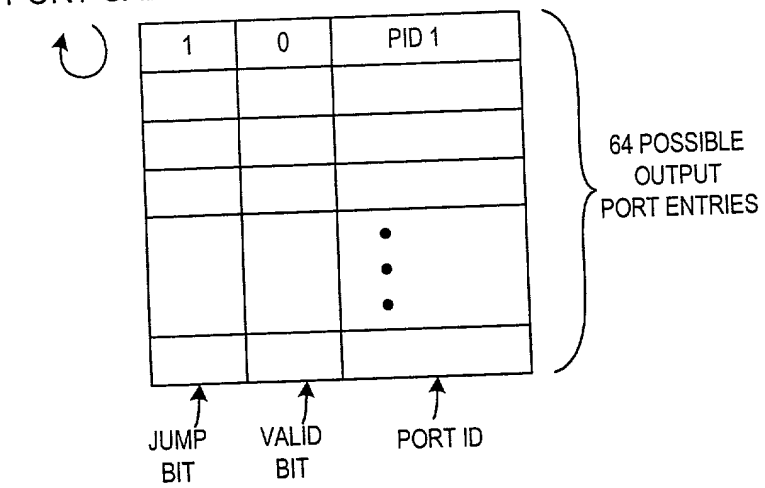


FIG. 24

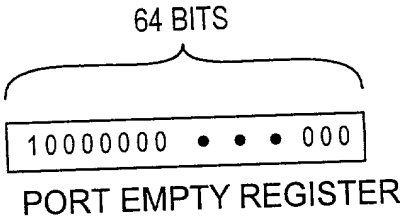


FIG. 25

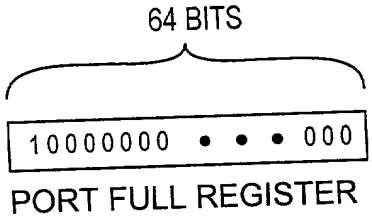
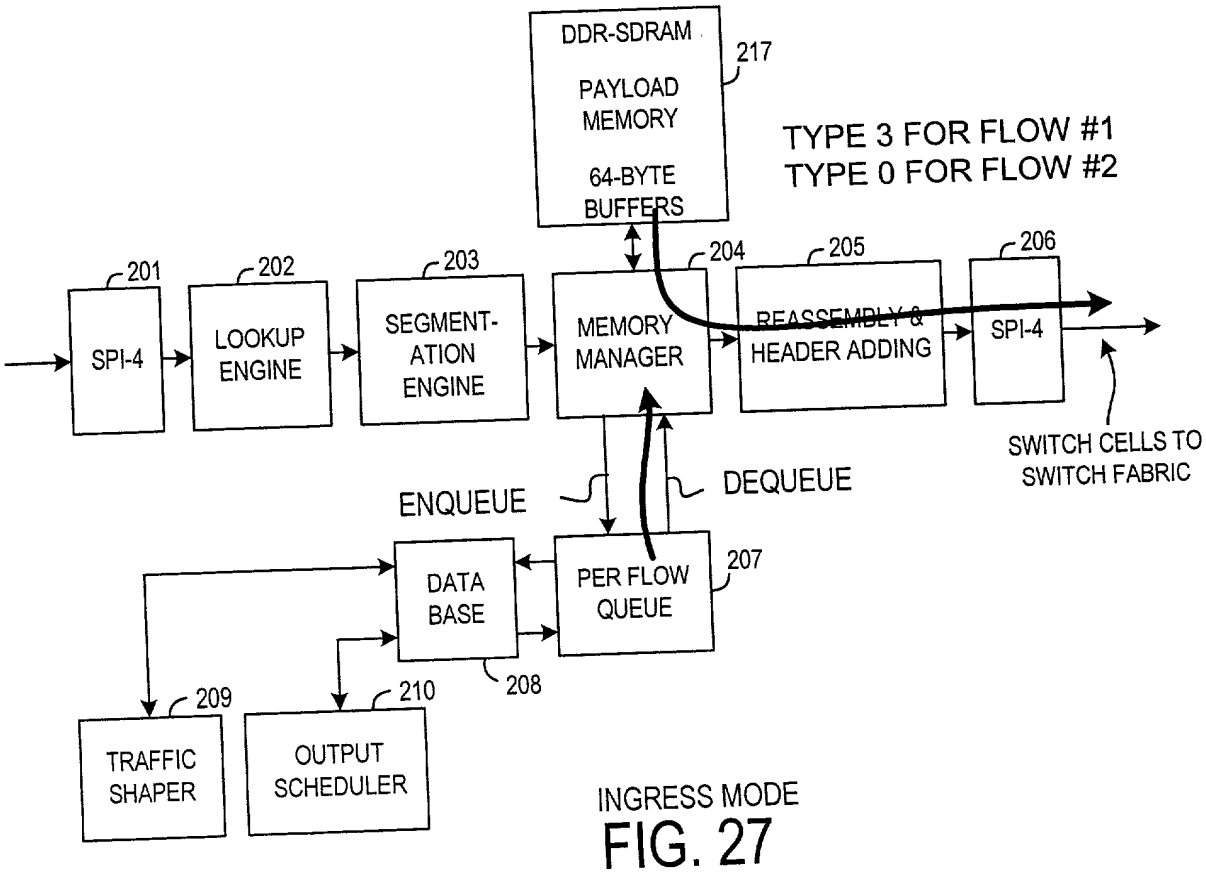


FIG. 26



INGRESS MODE

FIG. 27

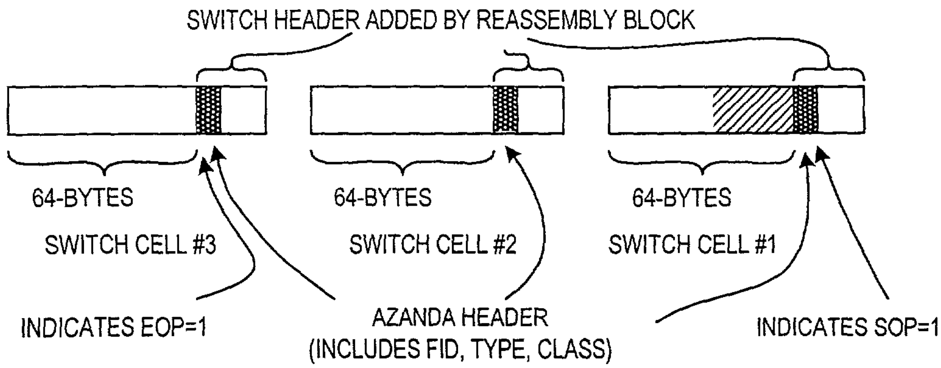


FIG. 28

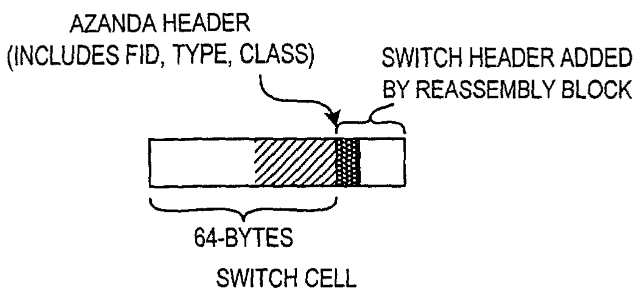


FIG. 29

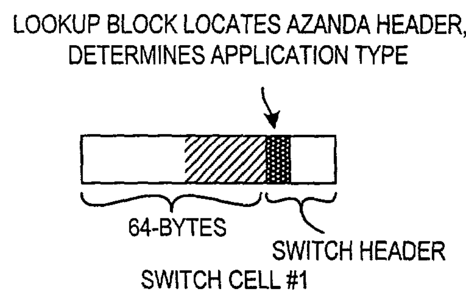
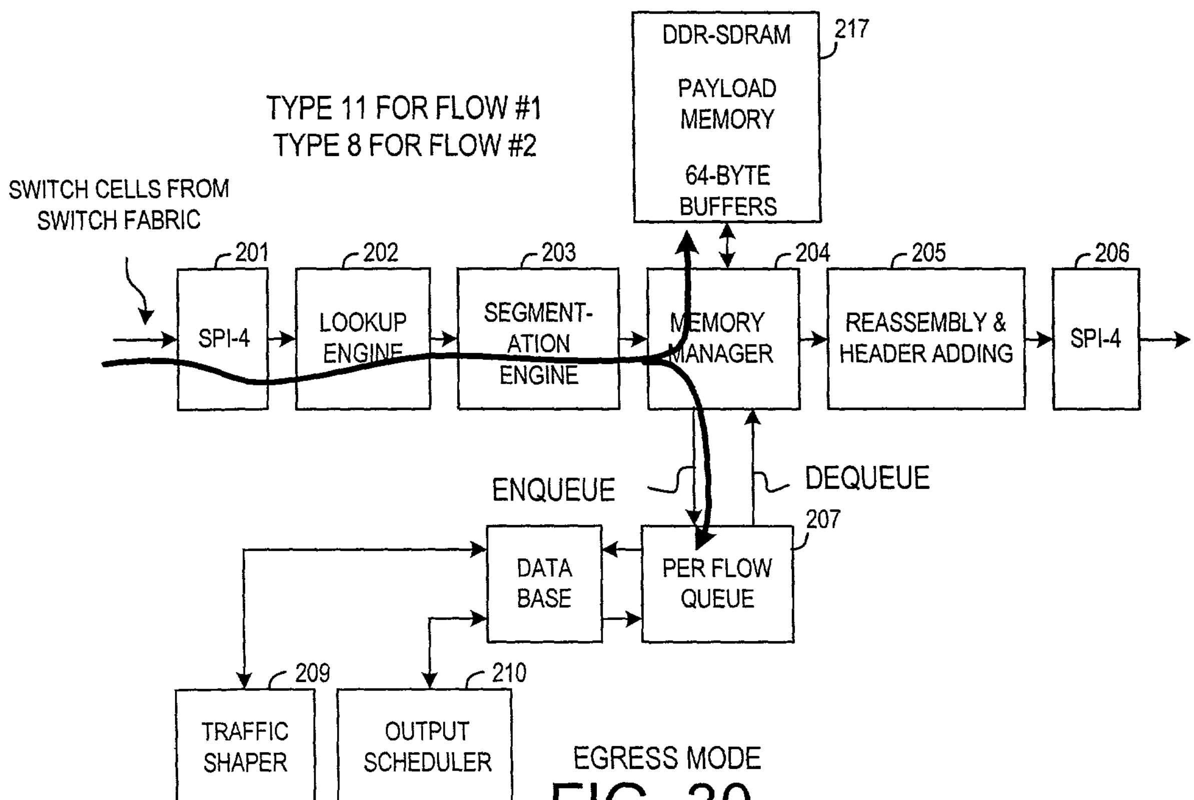
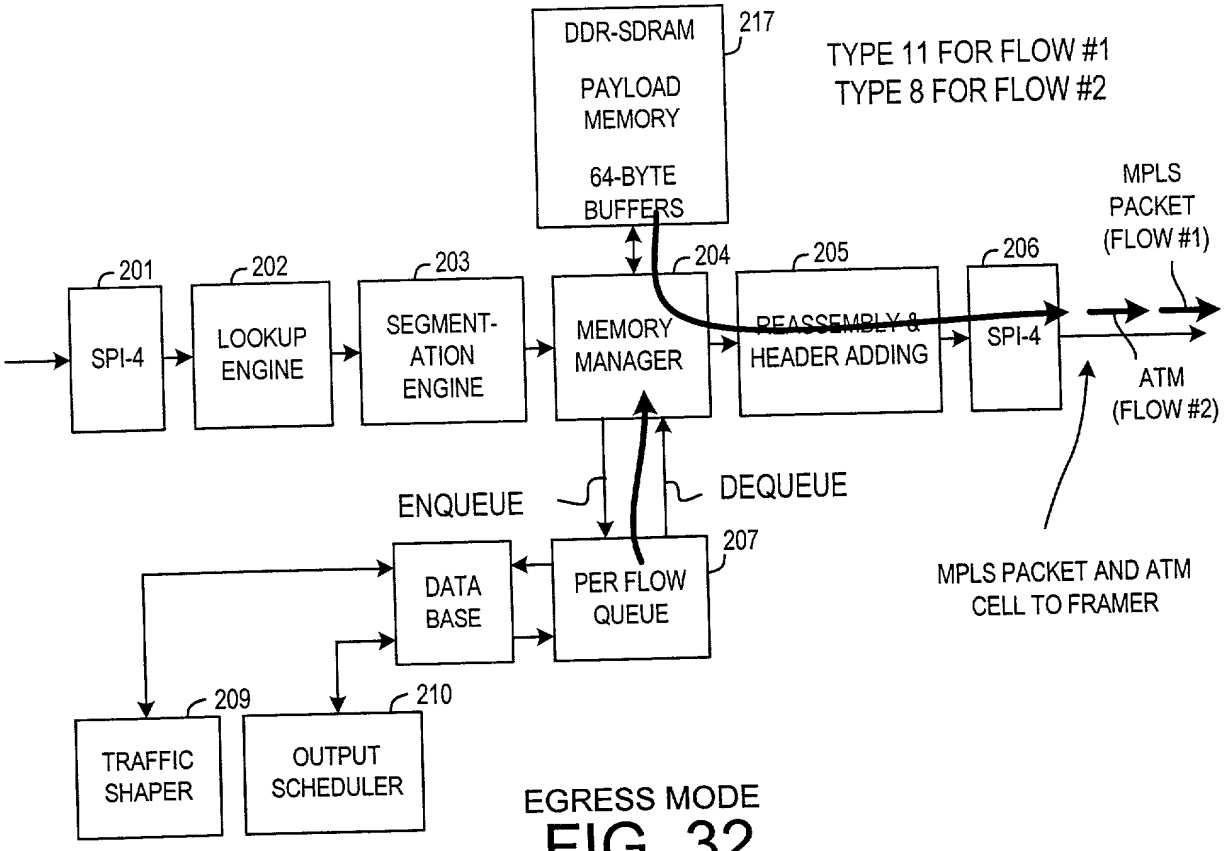


FIG. 31



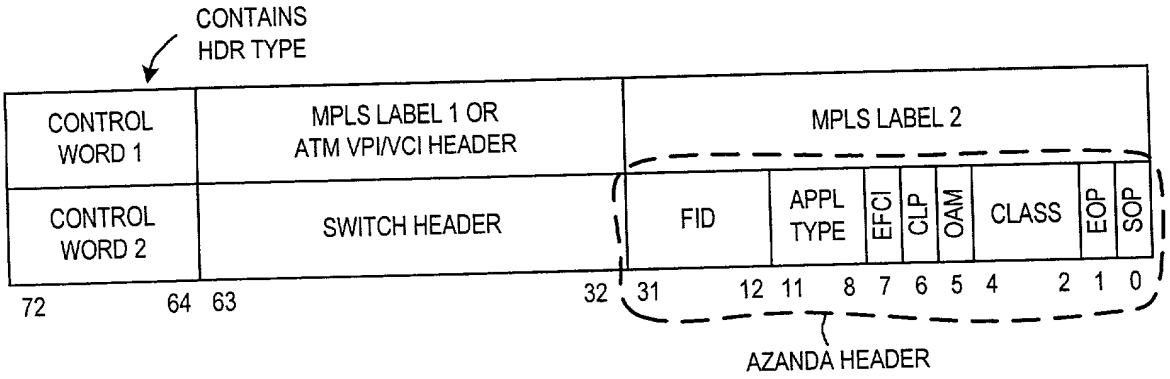
EGRESS MODE

FIG. 30



EGRESS MODE

FIG. 32



FORMAT OF ONE FID ENTRY IN HEADER TABLE

FIG. 33

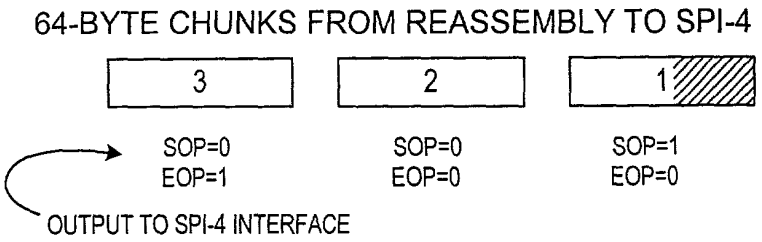


FIG. 34

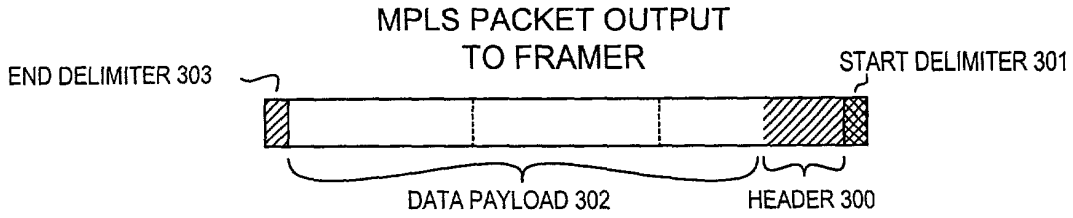


FIG. 35

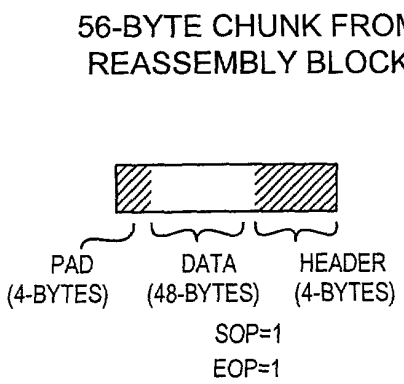


FIG. 36

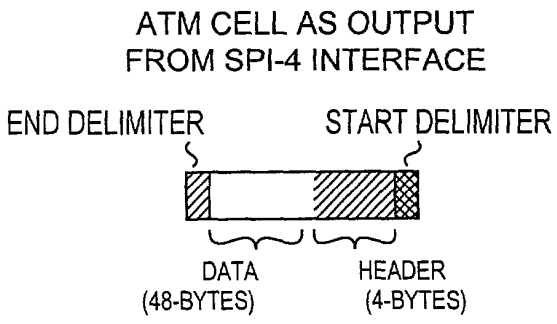


FIG. 37

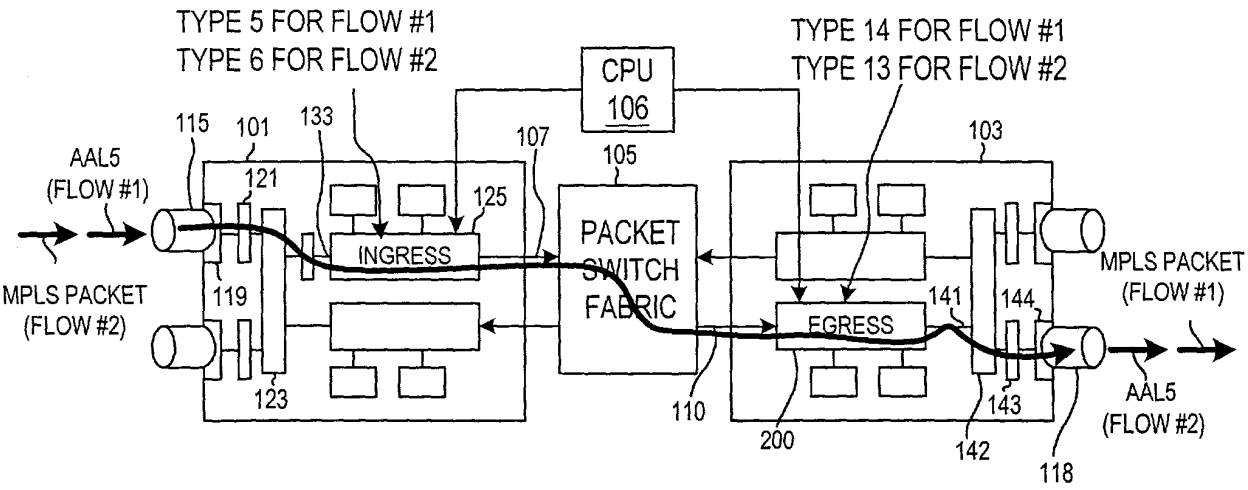
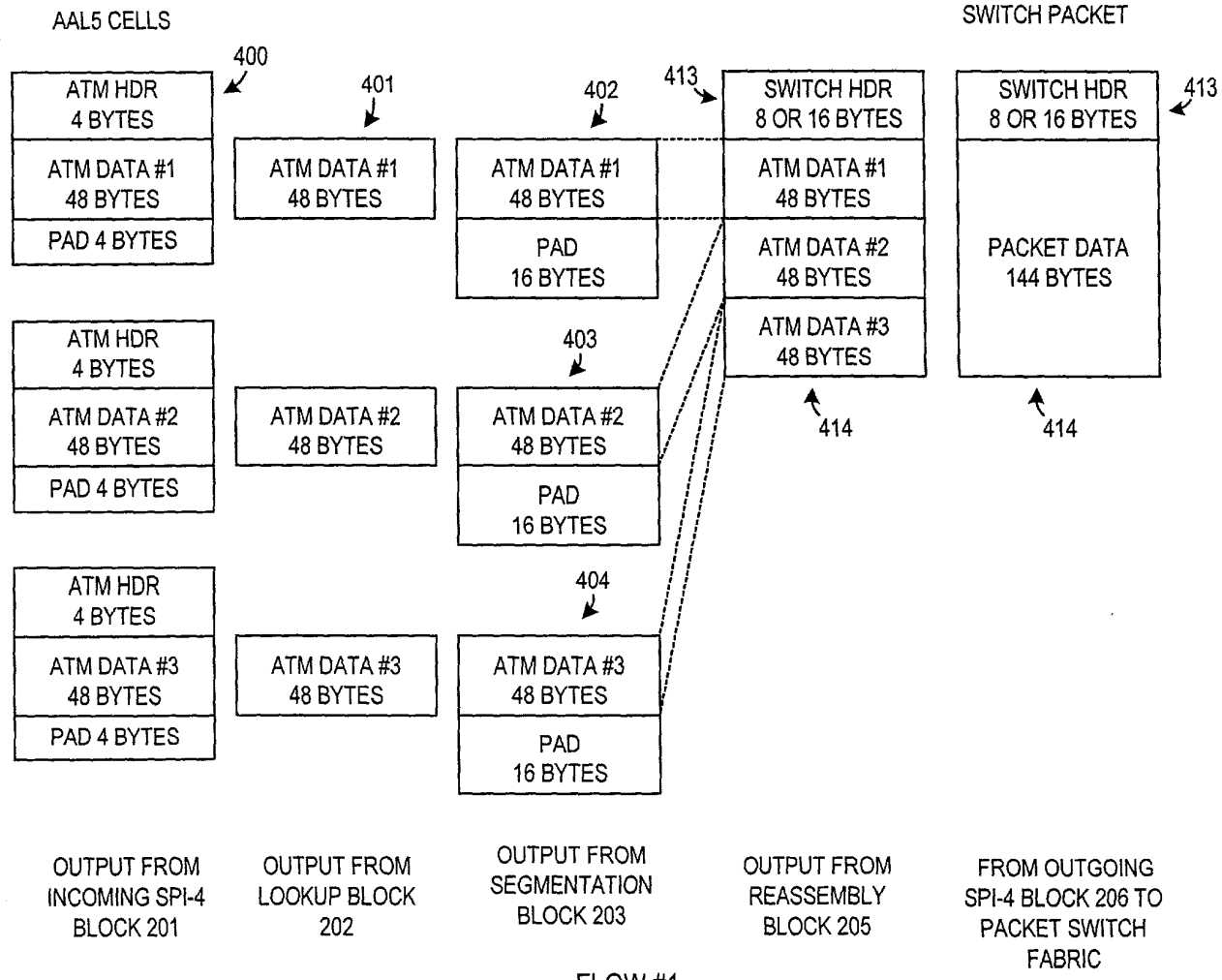


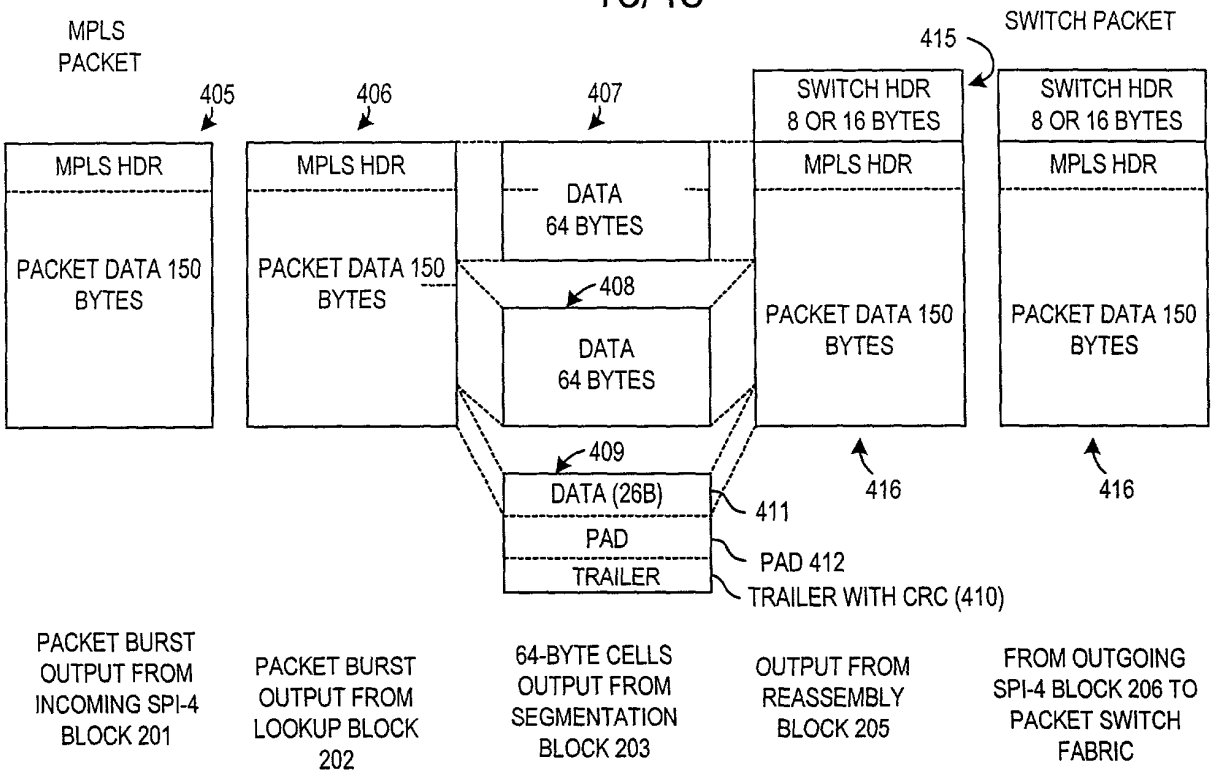
FIG. 38



FLOW #1

INGRESS APPLICATION TYPE 5

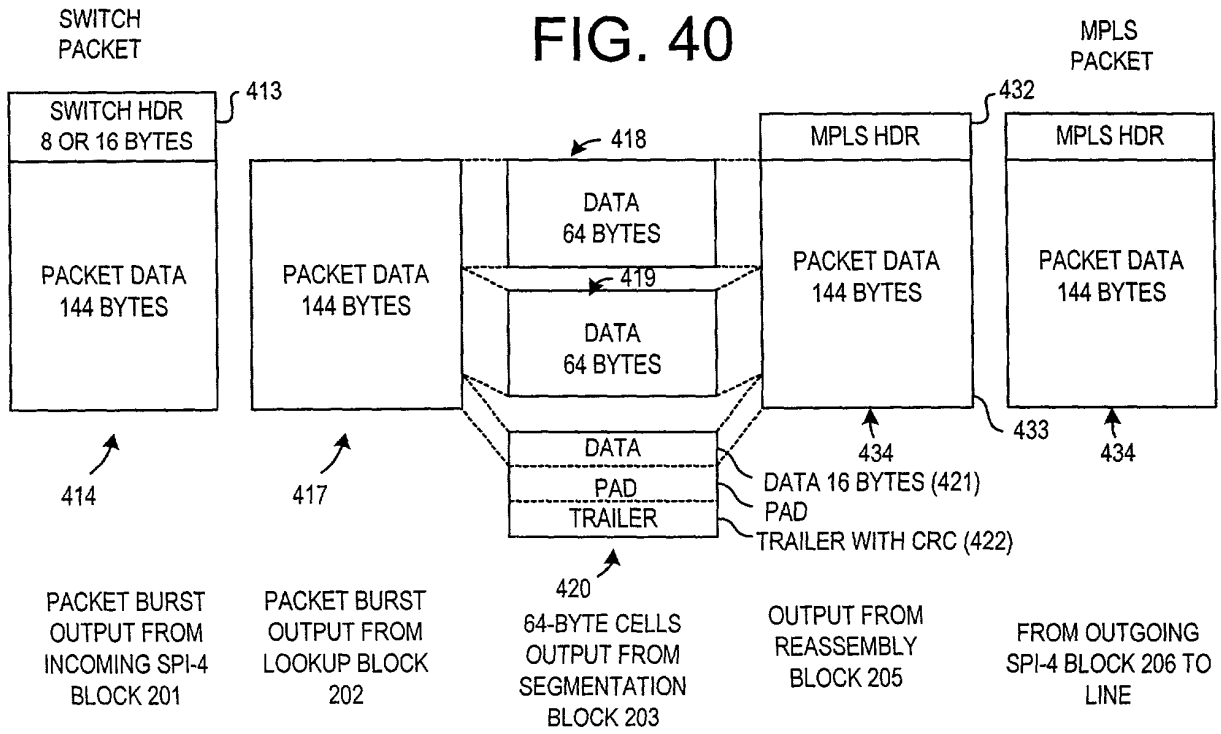
FIG. 39



FLOW #2

INGRESS APPLICATION TYPE 6

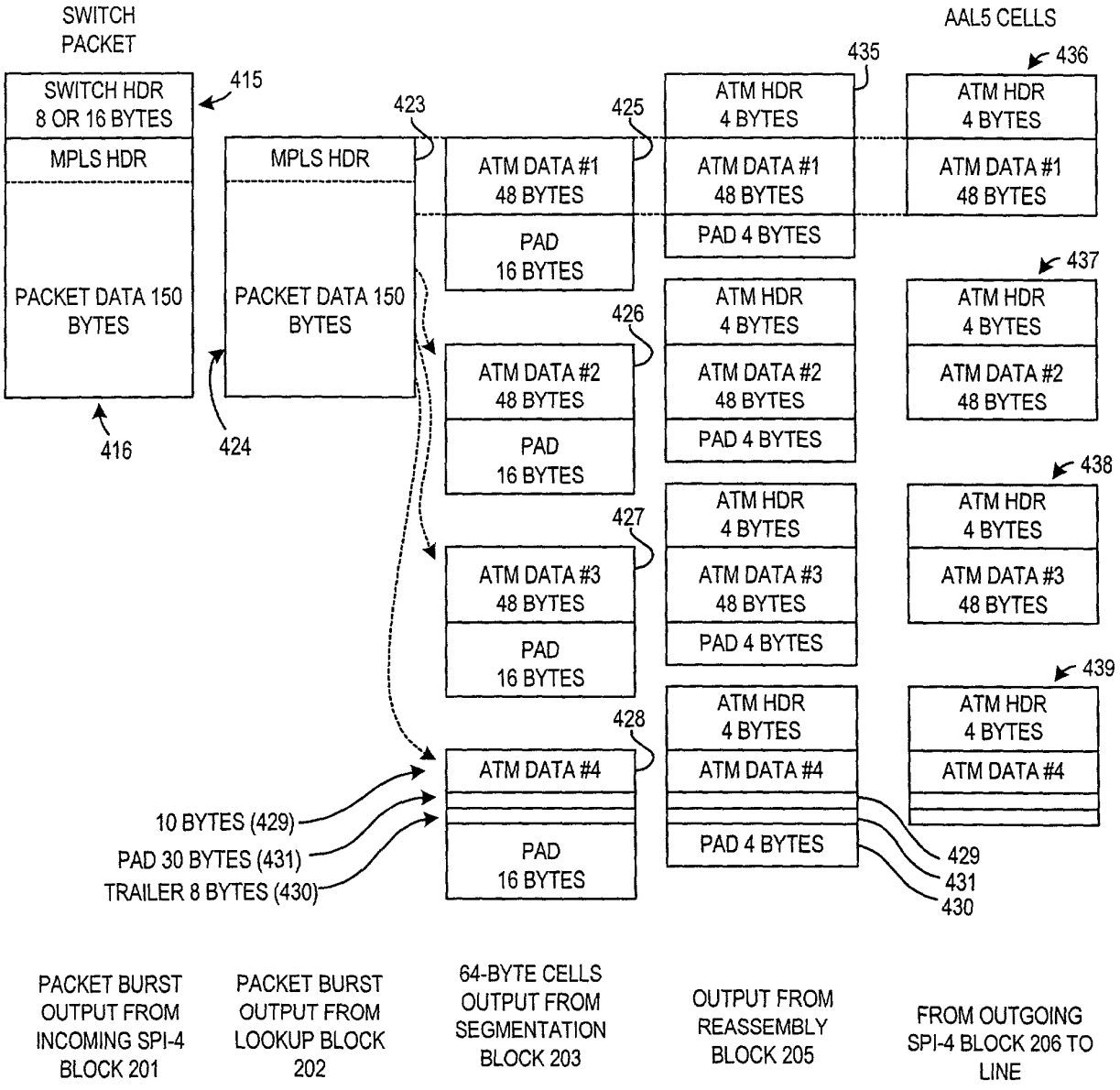
FIG. 40



FLOW #1

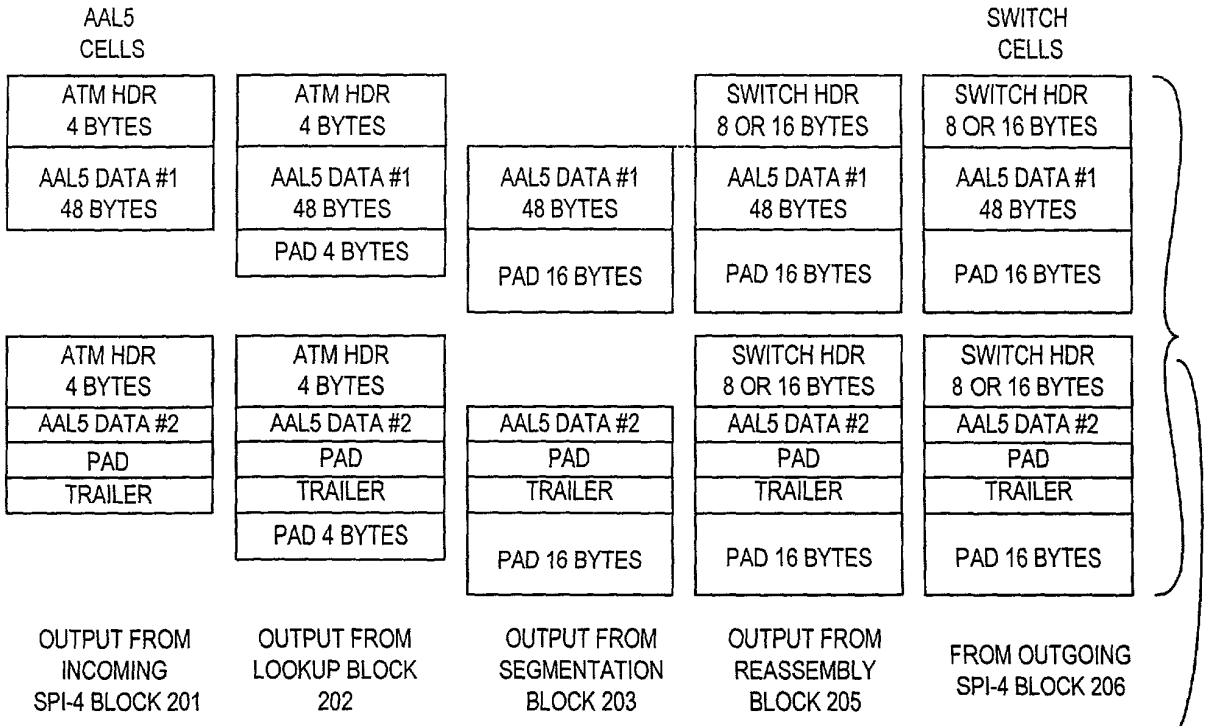
EGRESS APPLICATION TYPE 14

FIG. 41

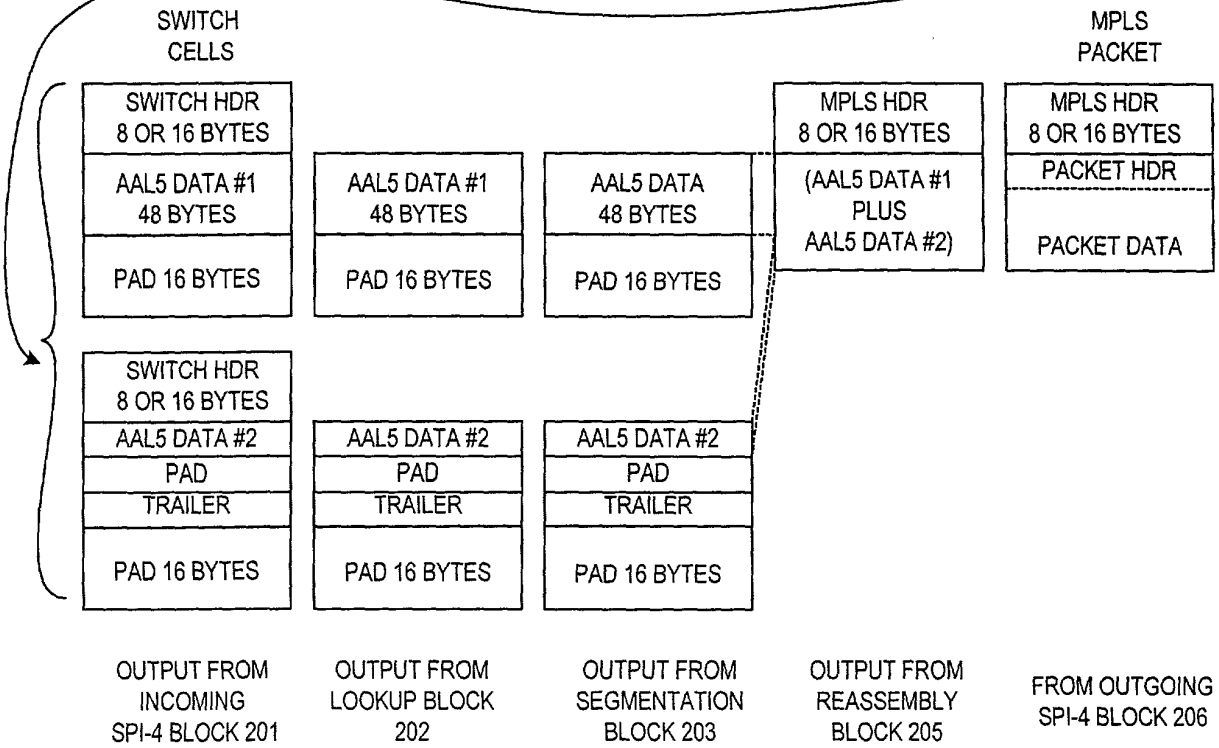


FLOW #2
EGRESS APPLICATION TYPE 13

FIG. 42



INGRESS APPLICATION TYPE 1



EGRESS APPLICATION TYPE 9

FIG. 43

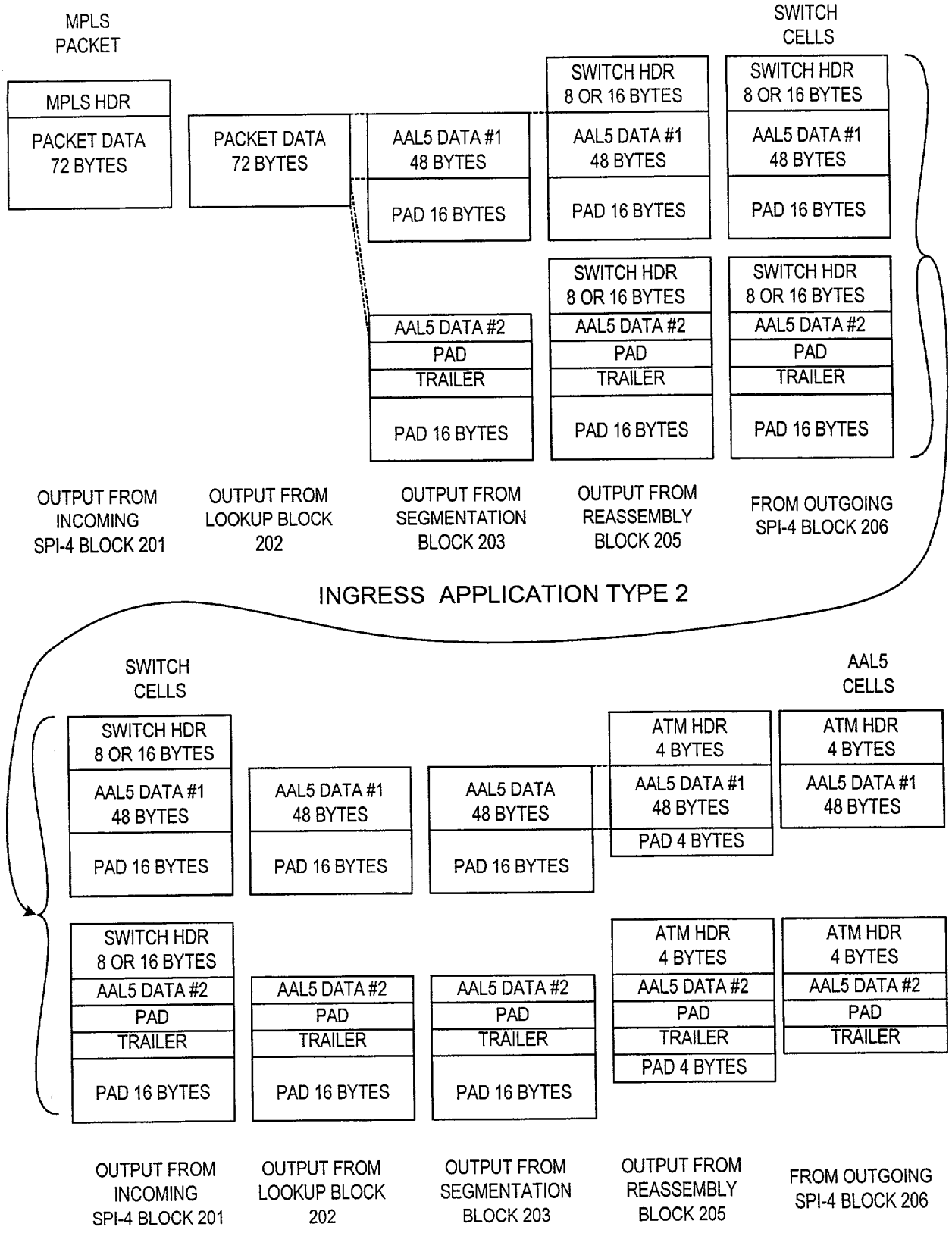

MPLS PACKET
MPLS HDR
PACKET DATA 72 BYTES
PACKET DATA 72 BYTES
AAL5 DATA #1 48 BYTES
PAD 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #1 48 BYTES
PAD 16 BYTES
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
SWITCH CELLS
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #1 48 BYTES
PAD 16 BYTES
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
INGRESS APPLICATION TYPE 2
SWITCH CELLS
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #1 48 BYTES
PAD 16 BYTES
SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
AAL5 DATA #1 48 BYTES
PAD 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
AAL5 DATA 48 BYTES
PAD 16 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 16 BYTES
ATM HDR 4 BYTES
AAL5 DATA #1 48 BYTES
PAD 4 BYTES
ATM HDR 4 BYTES
AAL5 DATA #2
PAD
TRAILER
PAD 4 BYTES
AAL5 CELLS
ATM HDR 4 BYTES
AAL5 DATA #1 48 BYTES
ATM HDR 4 BYTES
AAL5 DATA #2
PAD
TRAILER
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
EGRESS APPLICATION TYPE 10

FIG. 44

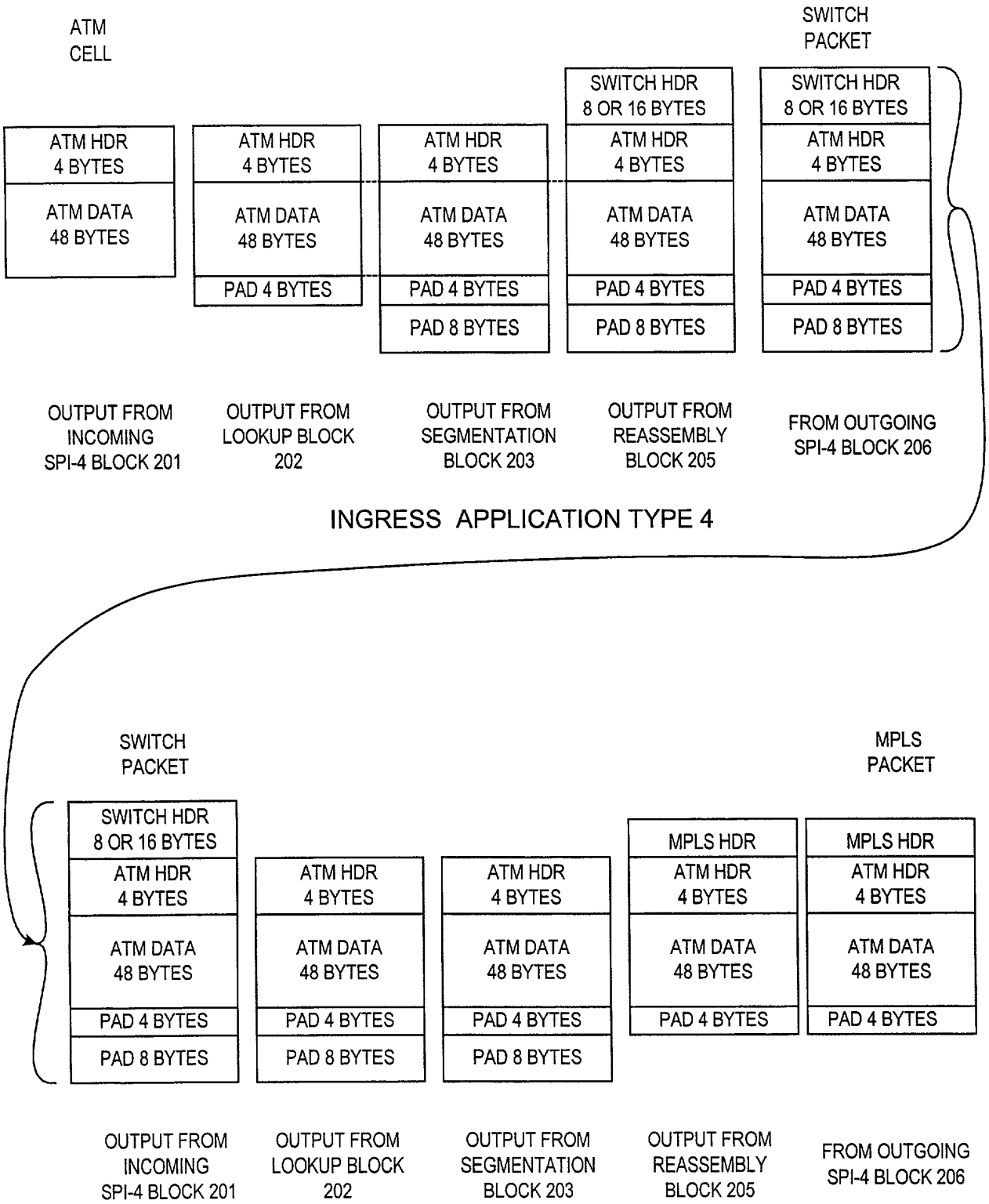

ATM CELL
SWITCH PACKET
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES
PAD 8 BYTES
SWITCH HDR 8 OR 16 BYTES
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
INGRESS APPLICATION TYPE 4
SWITCH PACKET
MPLS PACKET
MPLS HDR
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
EGRESS APPLICATION TYPE 14

FIG. 45

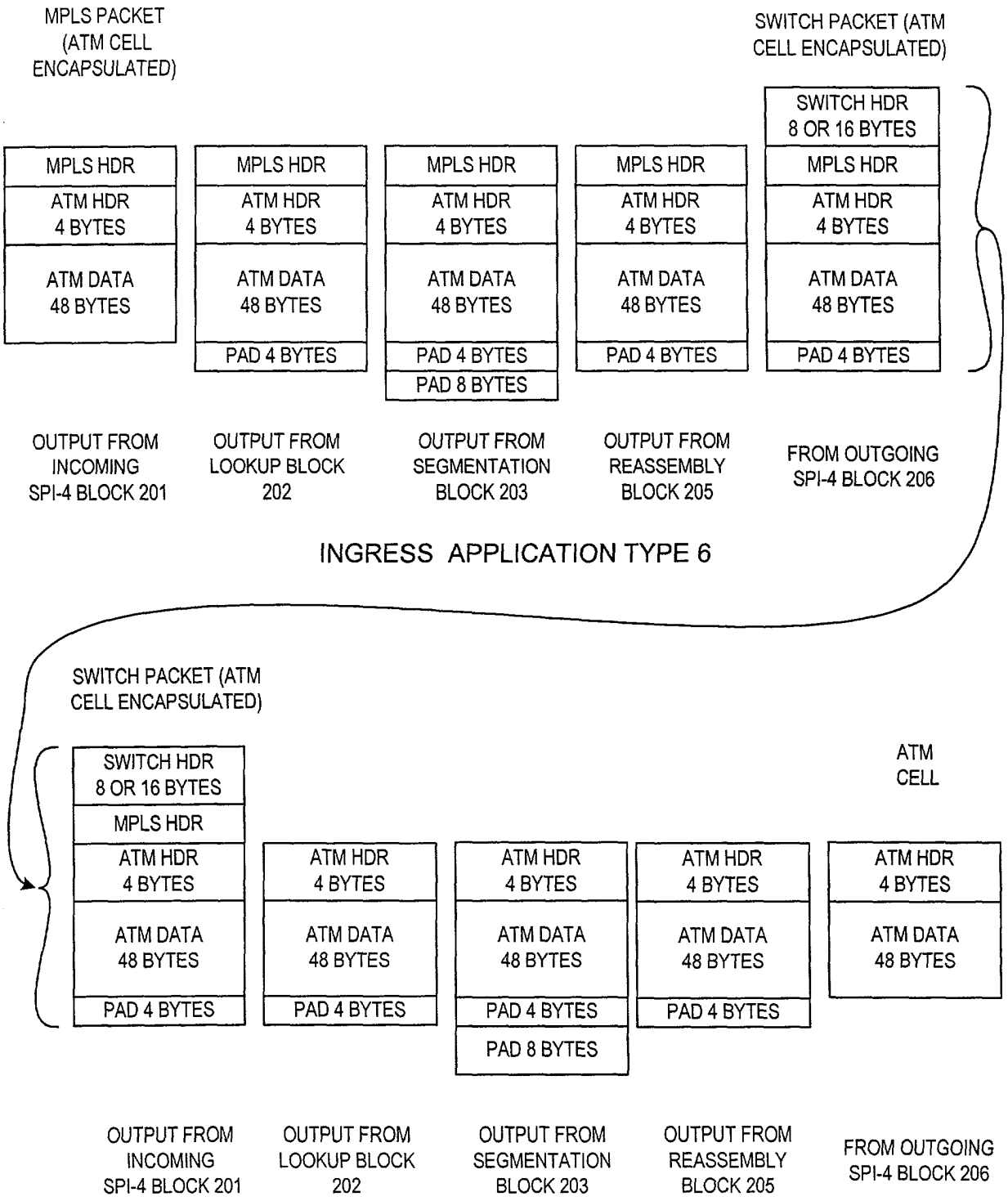

MPLS PACKET (ATM CELL ENCAPSULATED)
SWITCH PACKET (ATM CELL ENCAPSULATED)
SWITCH HDR 8 OR 16 BYTES
MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES
PAD 8 BYTES
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
INGRESS APPLICATION TYPE 6
SWITCH PACKET (ATM CELL ENCAPSULATED)
ATM CELL
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
EGRESS APPLICATION TYPE 12 (ATM DE-ENCAPSULATION)

FIG. 46

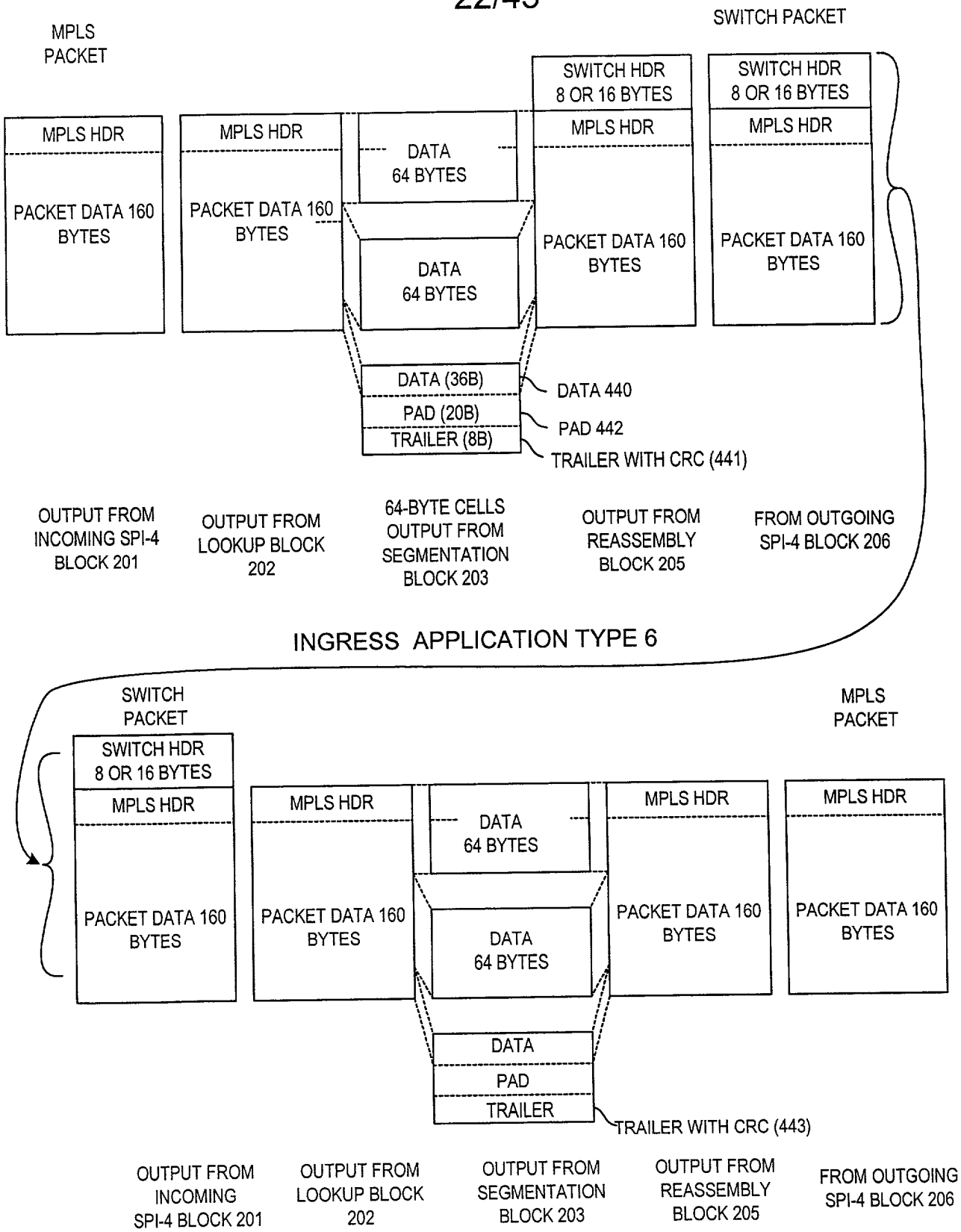

MPLS PACKET
SWITCH PACKET
MPLS HDR
PACKET DATA 160 BYTES
SWITCH HDR 8 OR 16 BYTES
DATA 64 BYTES
DATA (36B)
PAD (20B)
TRAILER (8B)
DATA 440
PAD 442
TRAILER WITH CRC (441)
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
64-BYTE CELLS OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
INGRESS APPLICATION TYPE 6
SWITCH PACKET
MPLS PACKET
DATA
PAD
TRAILER
TRAILER WITH CRC (443)
OUTPUT FROM INCOMING SPI-4 BLOCK 201
OUTPUT FROM LOOKUP BLOCK 202
OUTPUT FROM SEGMENTATION BLOCK 203
OUTPUT FROM REASSEMBLY BLOCK 205
FROM OUTGOING SPI-4 BLOCK 206
EGRESS APPLICATION TYPE 14

FIG. 47

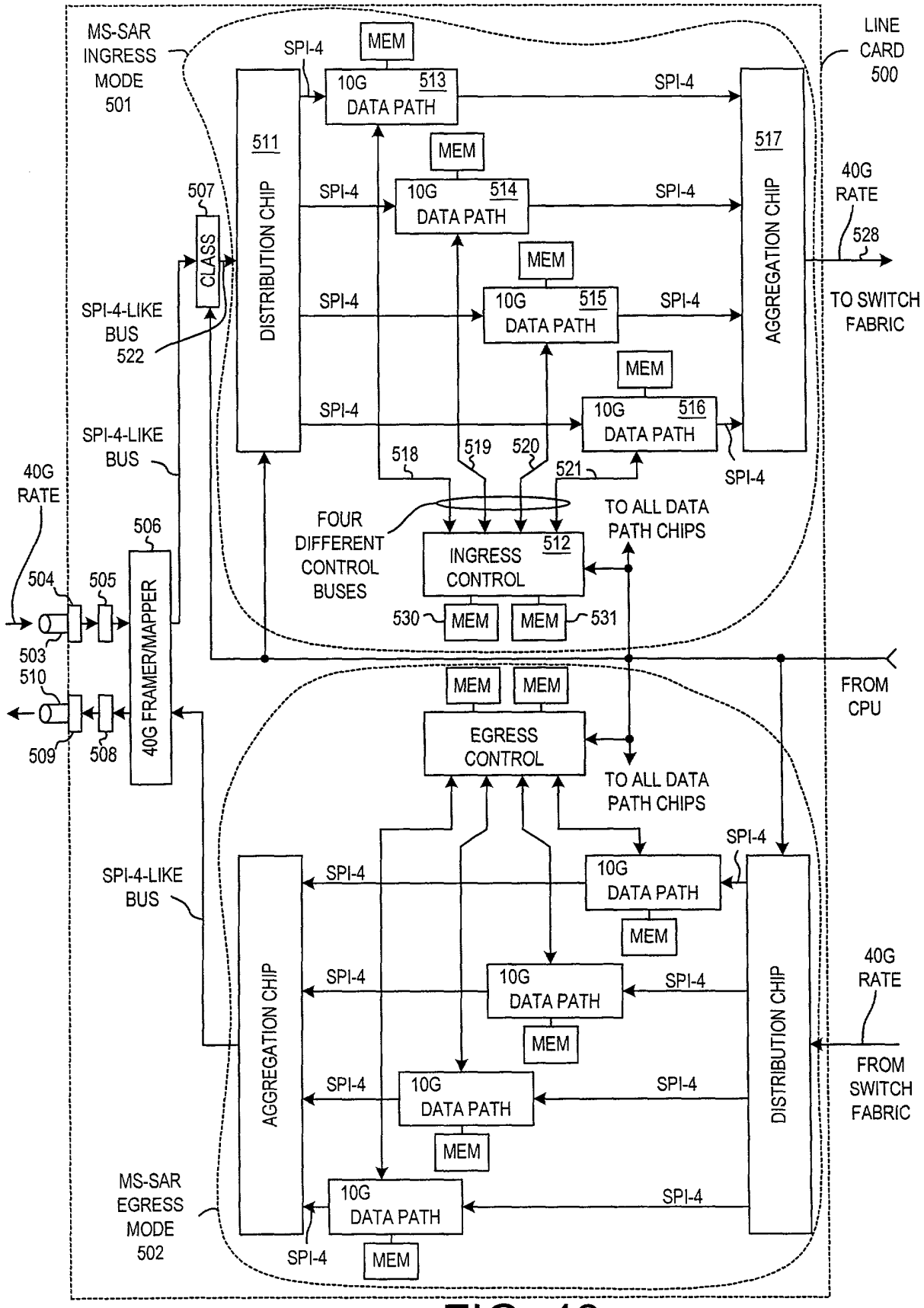

MS-SAR INGRESS MODE 501
LINE CARD 500
SPI-4
MEM
10G DATA PATH 513
10G DATA PATH 514
10G DATA PATH 515
10G DATA PATH 516
511
DISTRIBUTION CHIP
517
AGGREGATION CHIP
507
CLASS
SPI-4-LIKE BUS 522
40G RATE 528
TO SWITCH FABRIC
SPI-4-LIKE BUS
40G RATE
504
505
506
503
510
509
508
40G FRAMER/MAPPER
518
519
520
521
FOUR DIFFERENT CONTROL BUSES
INGRESS CONTROL 512
TO ALL DATA PATH CHIPS
530
531
FROM CPU
EGRESS CONTROL
TO ALL DATA PATH CHIPS
SPI-4-LIKE BUS
AGGREGATION CHIP
DISTRIBUTION CHIP
40G RATE
FROM SWITCH FABRIC
MS-SAR EGRESS MODE 502

FIG. 48

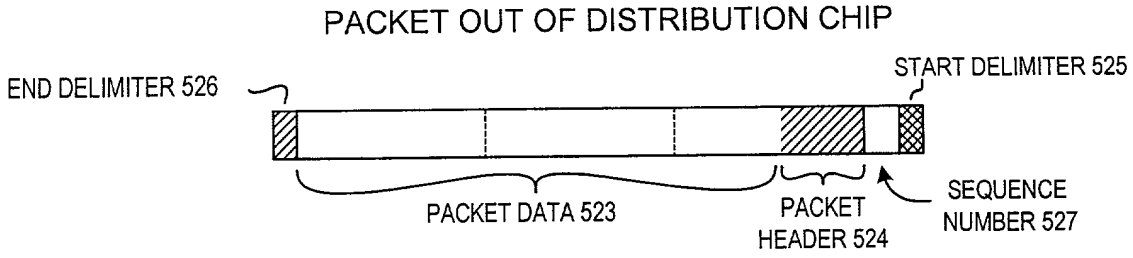
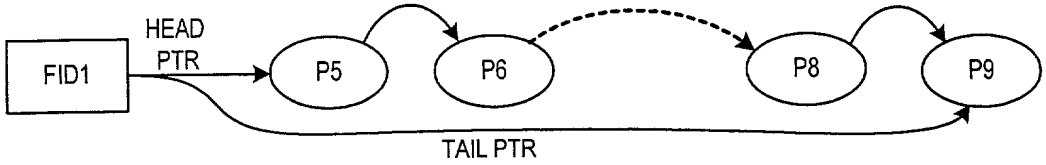
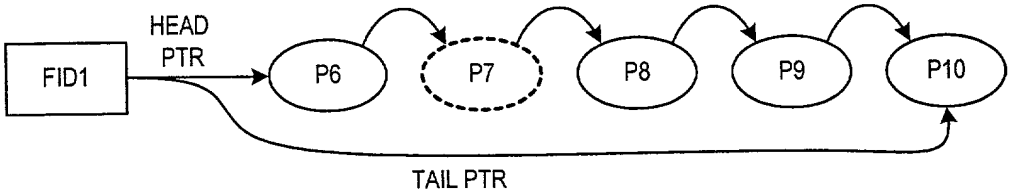


FIG. 49



PACKET QUEUE

FIG. 50



PACKET QUEUE

FIG. 51

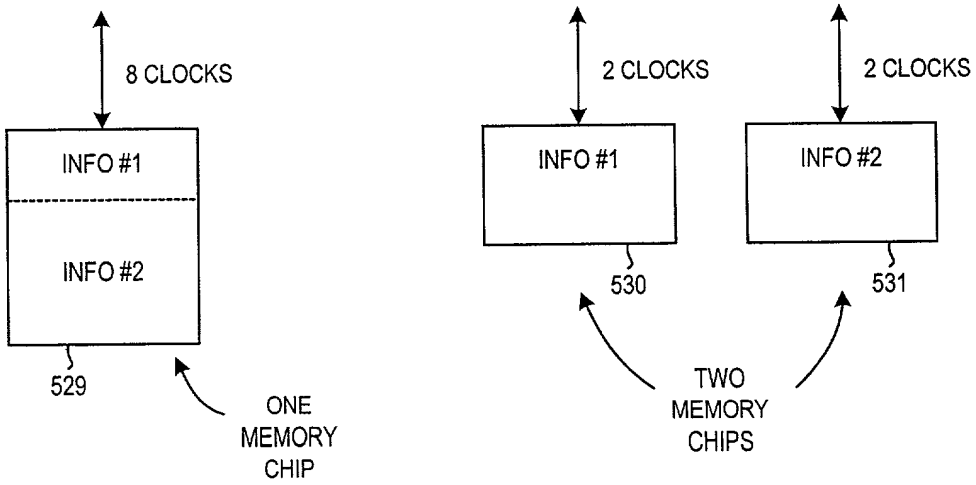


FIG. 52

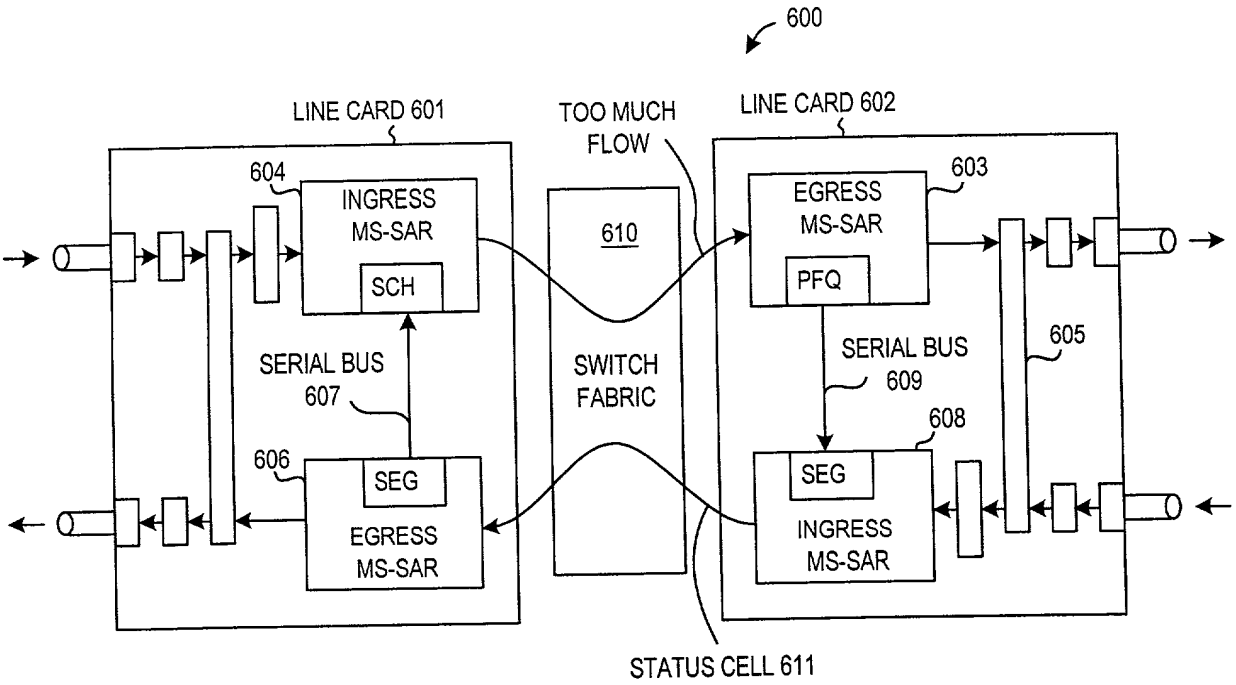


FIG. 53

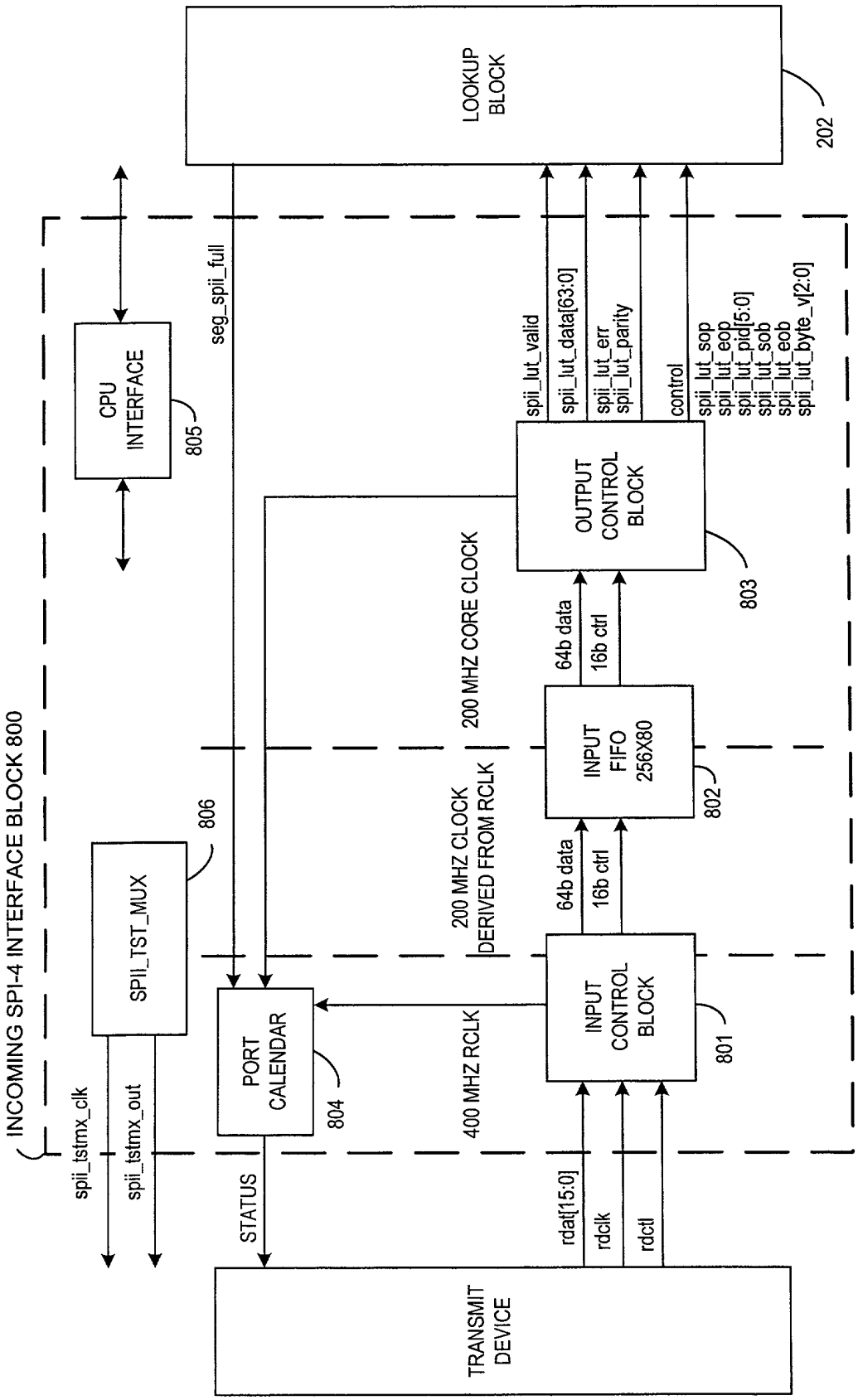
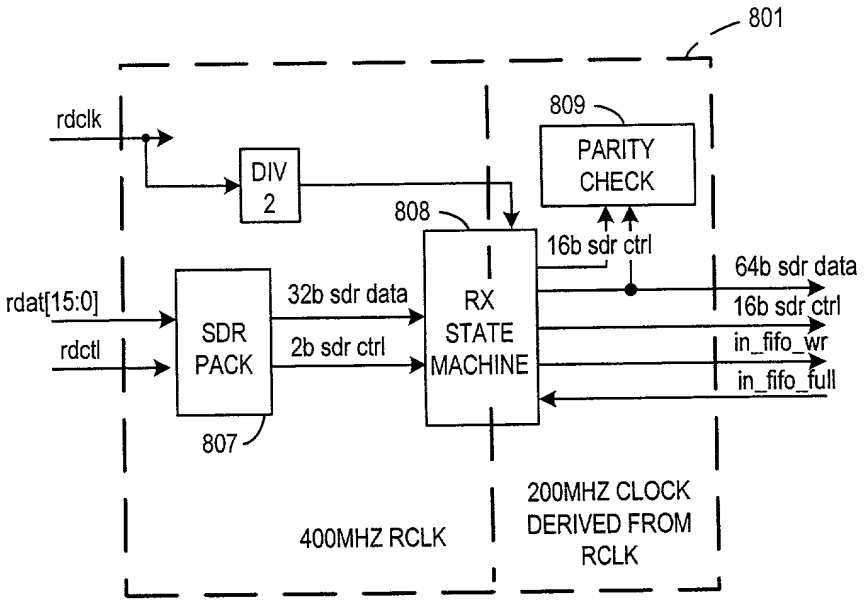
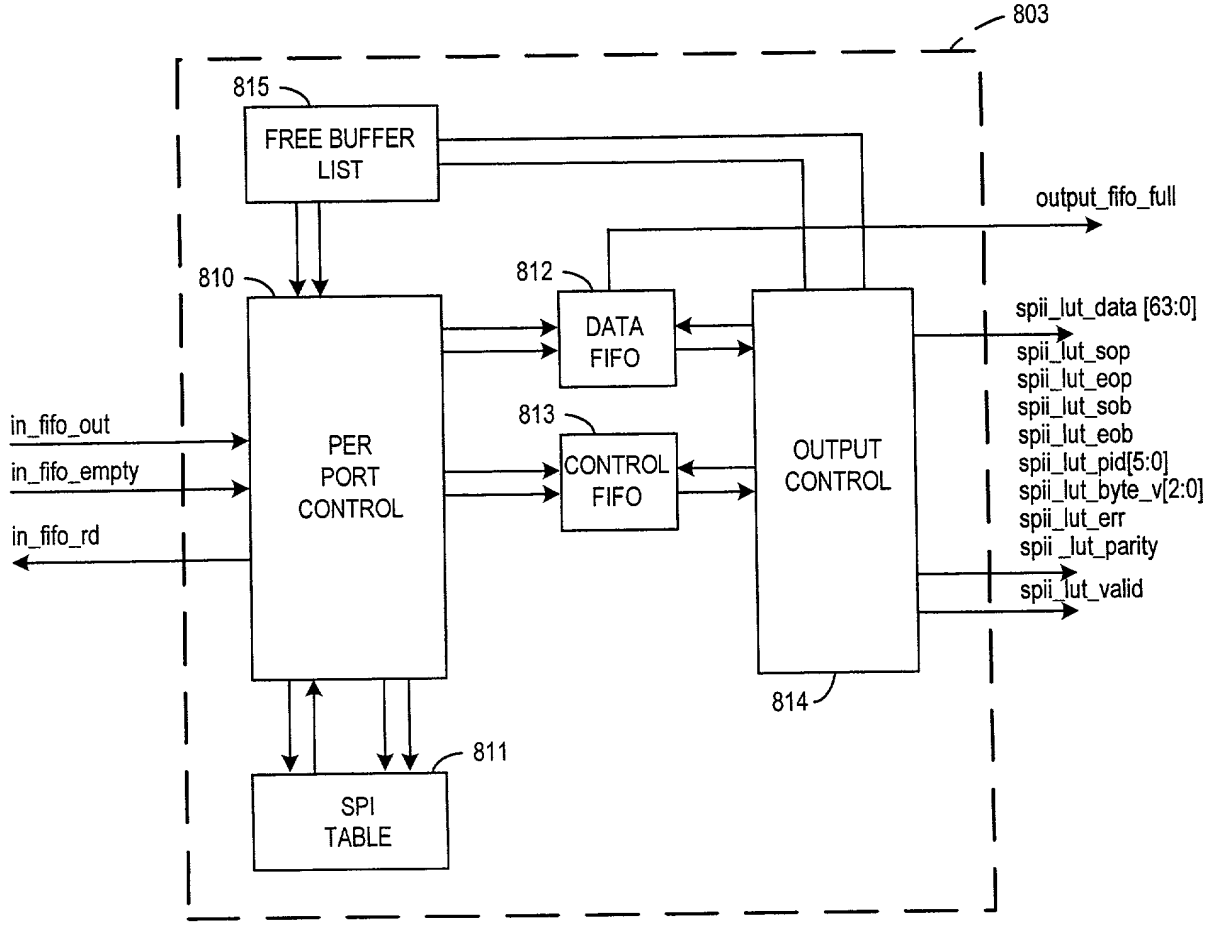

INCOMING SPI-4 INTERFACE BLOCK 800
LOOKUP BLOCK
202
CPU INTERFACE
805
seg_spii_full
spii_lut_valid
spii_lut_data[63:0]
spii_lut_err
spii_lut_parity
control
spii_lut_sop
spii_lut_eop
spii_lut_pid[5:0]
spii_lut_sob
spii_lut_eob
spii_lut_byte_v[2:0]
OUTPUT CONTROL BLOCK
803
200 MHZ CORE CLOCK
64b data
16b ctrl
INPUT FIFO 256X80
802
200 MHZ CLOCK DERIVED FROM RCLK
SPII_TST_MUX
806
PORT CALENDAR
804
400 MHZ RCLK
INPUT CONTROL BLOCK
801
spii_tstmx_clk
spii_tstmx_out
STATUS
rdat[15:0]
rdclk
rdctl
TRANSMIT DEVICE

FIG. 54



INPUT CONTROL BLOCK

FIG. 55



OUTPUT CONTROL BLOCK

FIG. 56

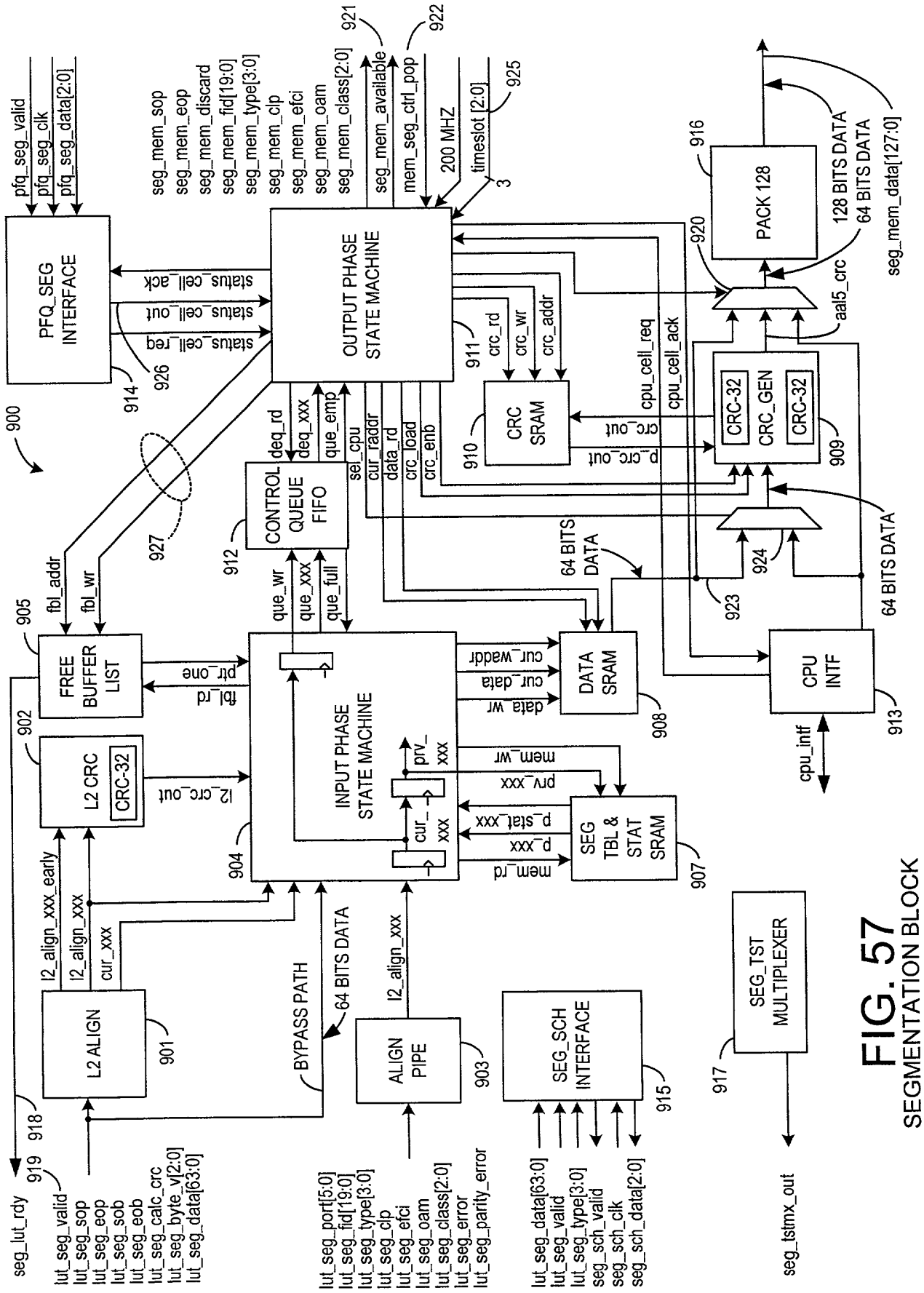


FIG. 57
SEGMENTATION BLOCK

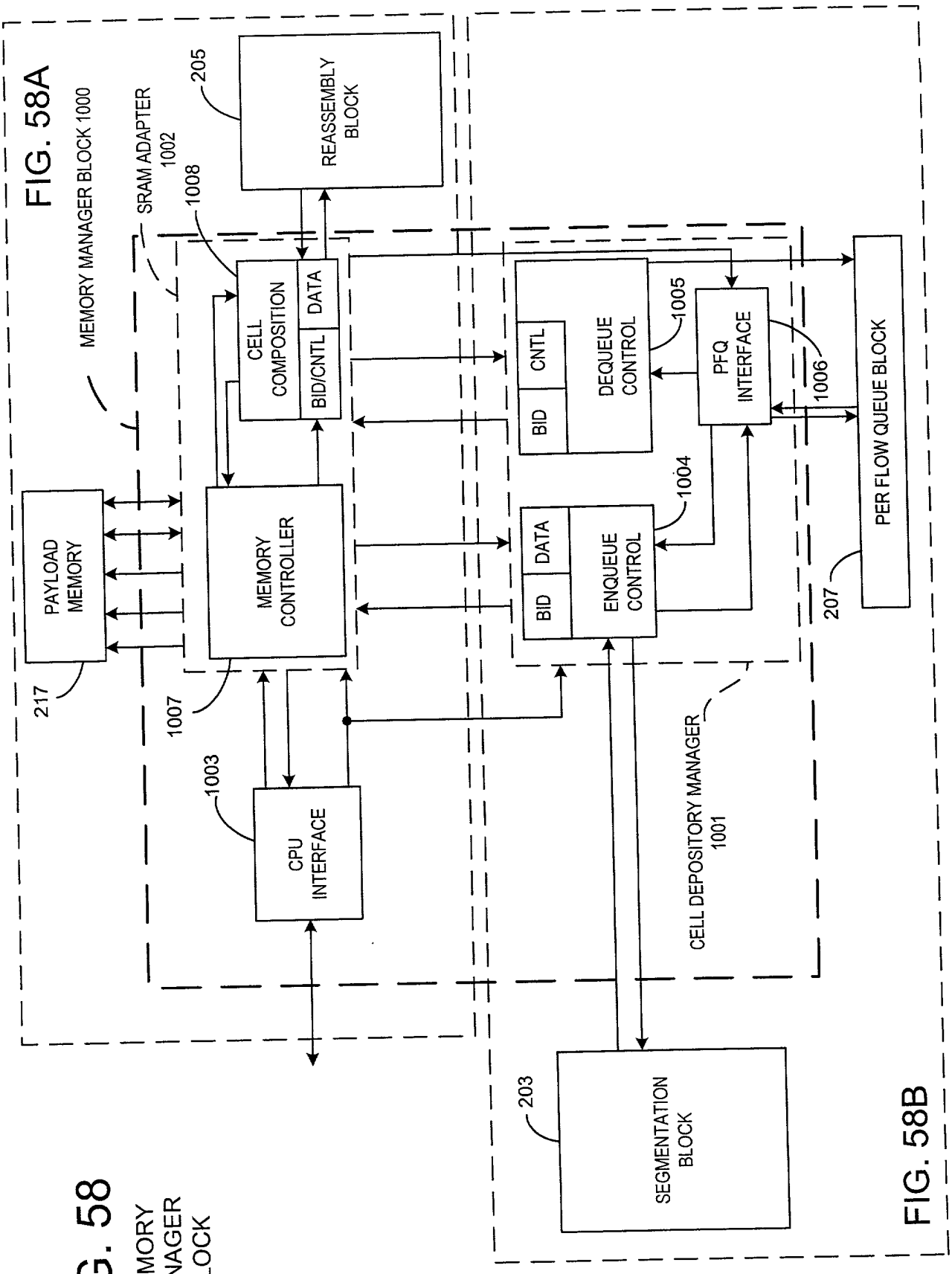
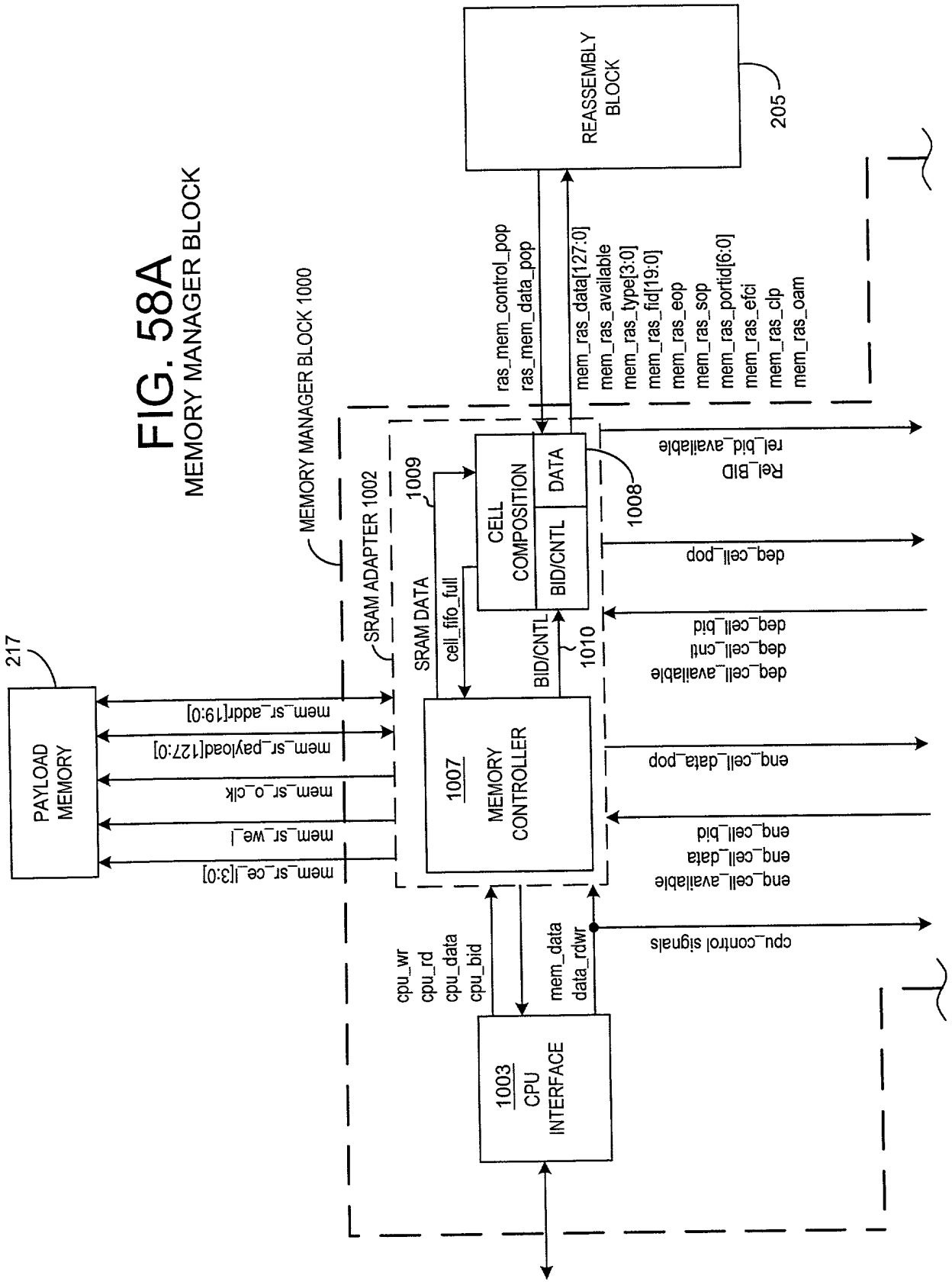


FIG. 58
MEMORY MANAGER BLOCK

FIG. 58A
MEMORY MANAGER BLOCK



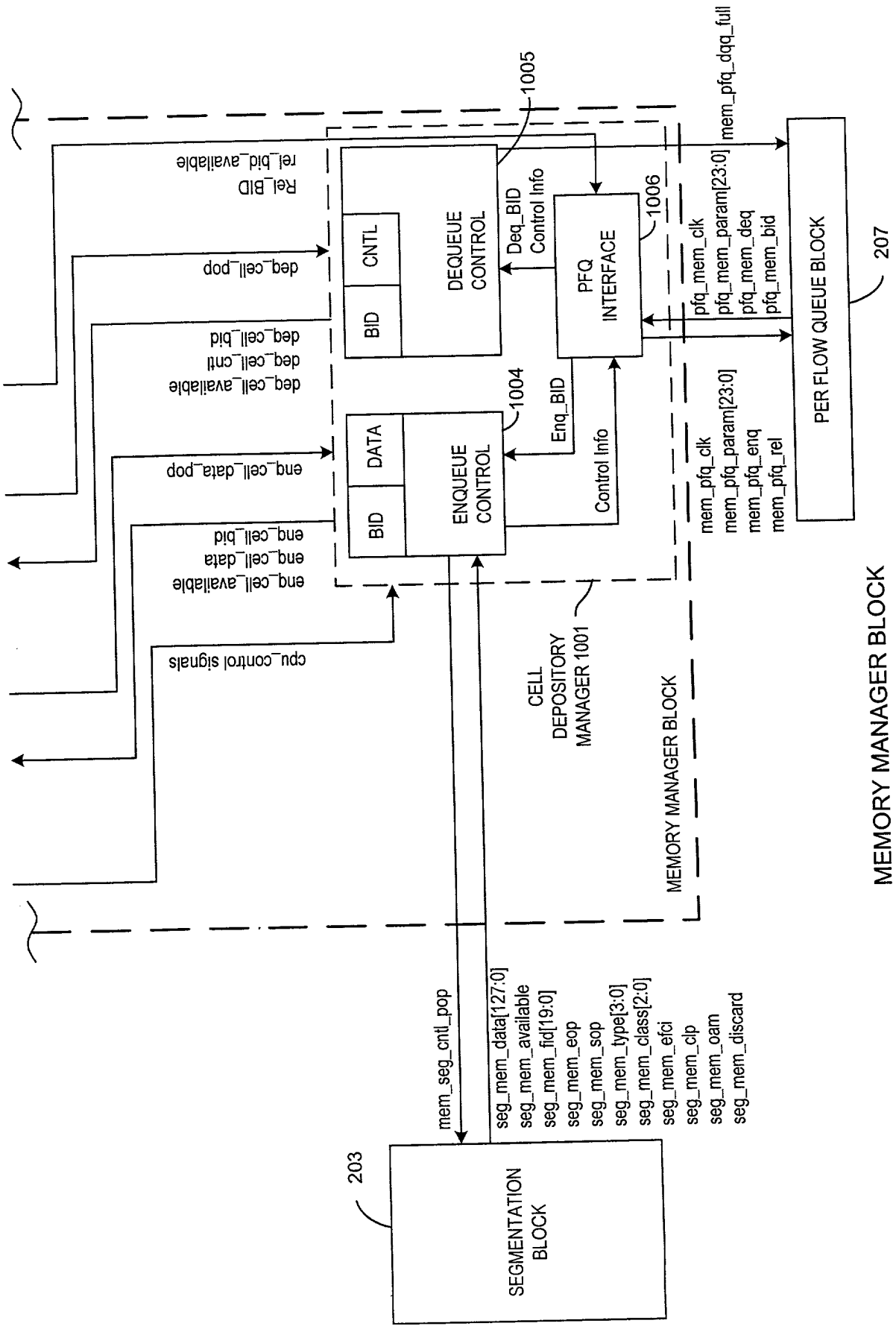

MEMORY MANAGER BLOCK
CELL DEPOSITORY MANAGER 1001
MEMORY MANAGER BLOCK
SEGMENTATION BLOCK
203
PER FLOW QUEUE BLOCK
207
ENQUEUE CONTROL
1004
DEQUEUE CONTROL
1005
PFQ INTERFACE
1006
DATA
BID
CNTL
BID
mem_seg_cntl_pop
seg_mem_data[127:0]
seg_mem_available
seg_mem_fid[19:0]
seg_mem_eop
seg_mem_sop
seg_mem_type[3:0]
seg_mem_class[2:0]
seg_mem_efci
seg_mem_clp
seg_mem_oam
seg_mem_discard
cpu_control signals
enq_cell_available
enq_cell_data
enq_cell_bid
enq_cell_data_pop
deq_cell_available
deq_cell_cnt
deq_cell_bid
deq_cell_pop
Rel_BID
rel_bid_available
Enq_BID
Control Info
Deq_BID
Control Info
mem_pfq_clk
mem_pfq_param[23:0]
mem_pfq_enq
mem_pfq_rel
pfq_mem_clk
pfq_mem_param[23:0]
pfq_mem_deq
pfq_mem_bid
mem_pfq_dqq_full

FIG. 58B

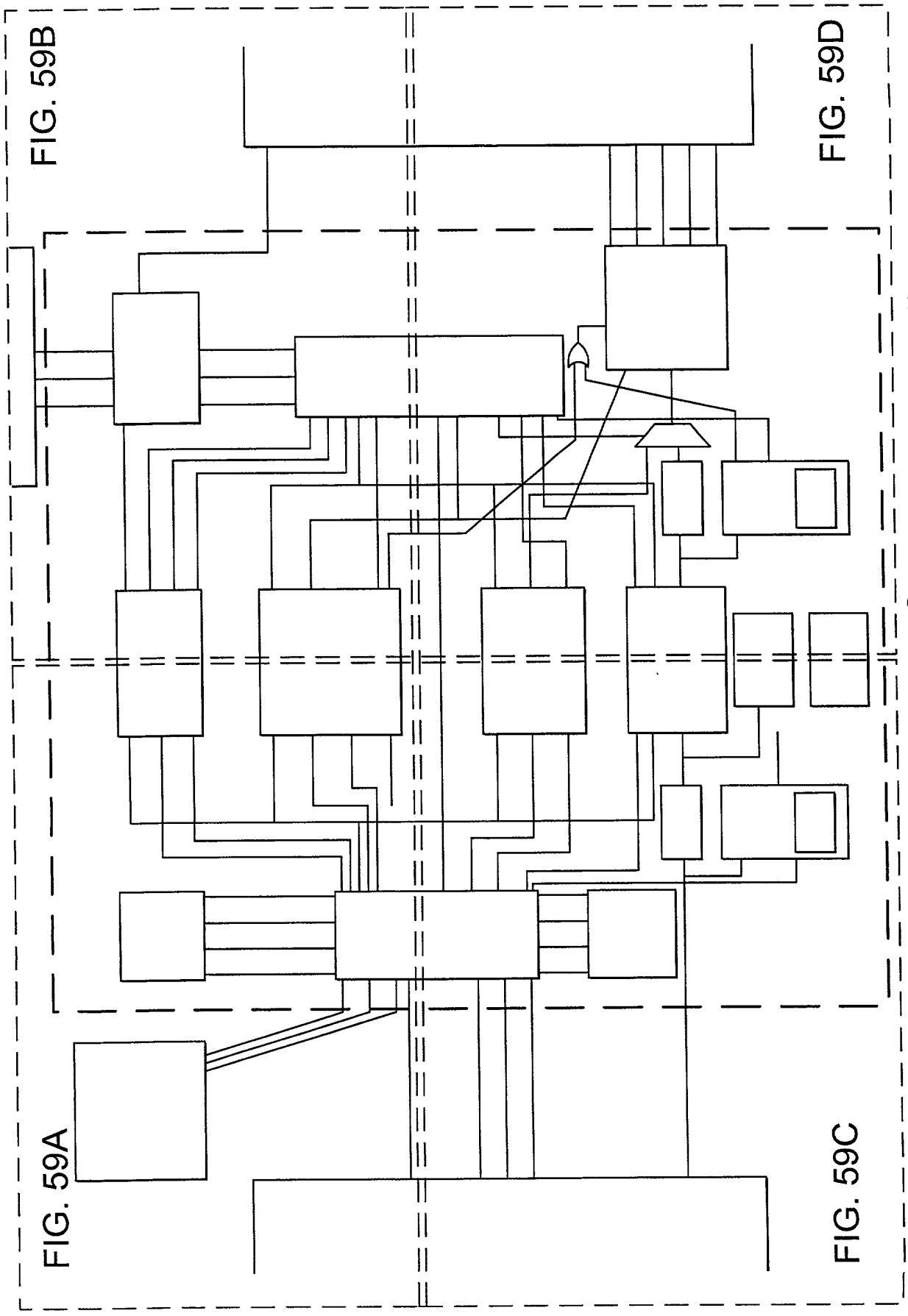


FIG. 59

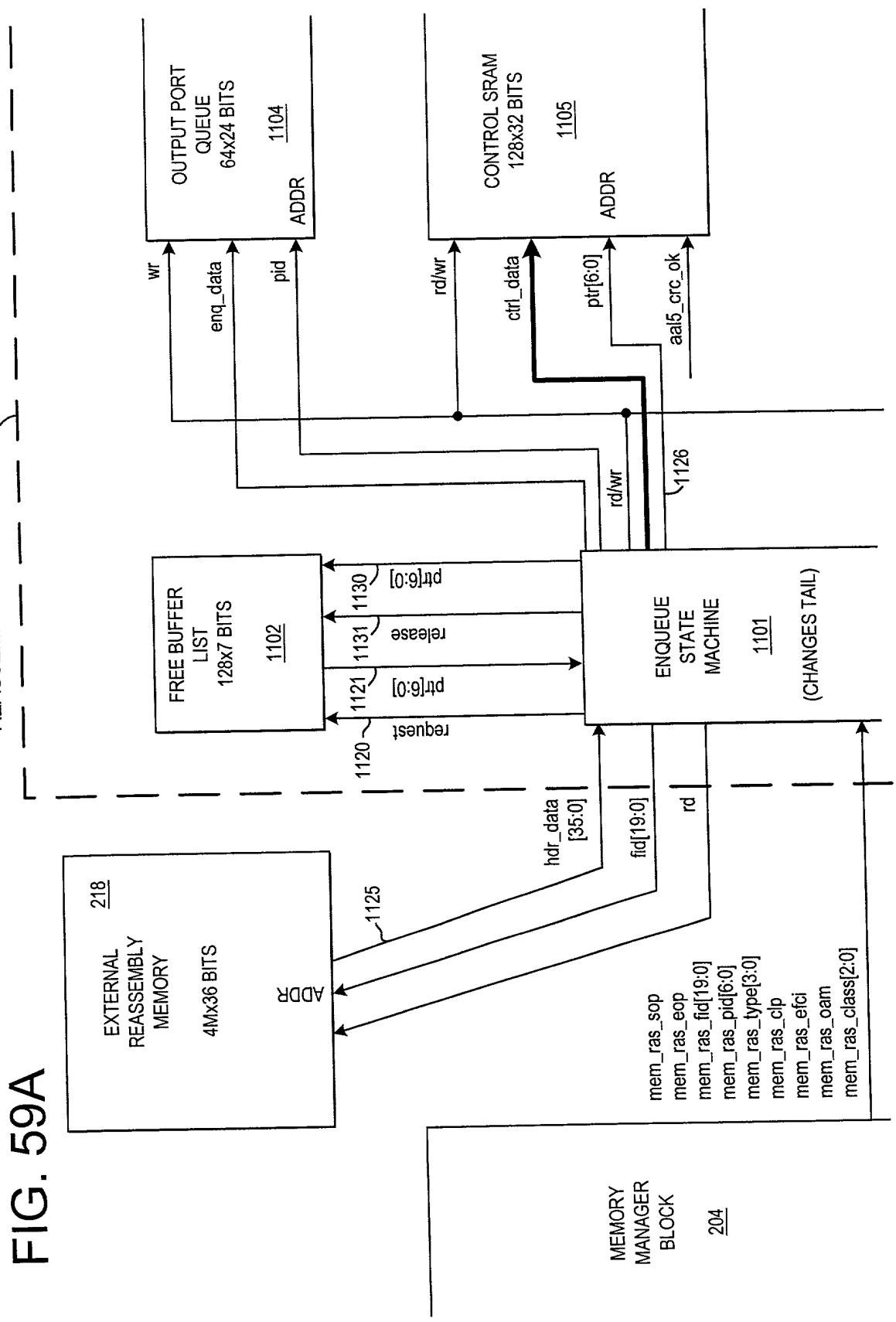
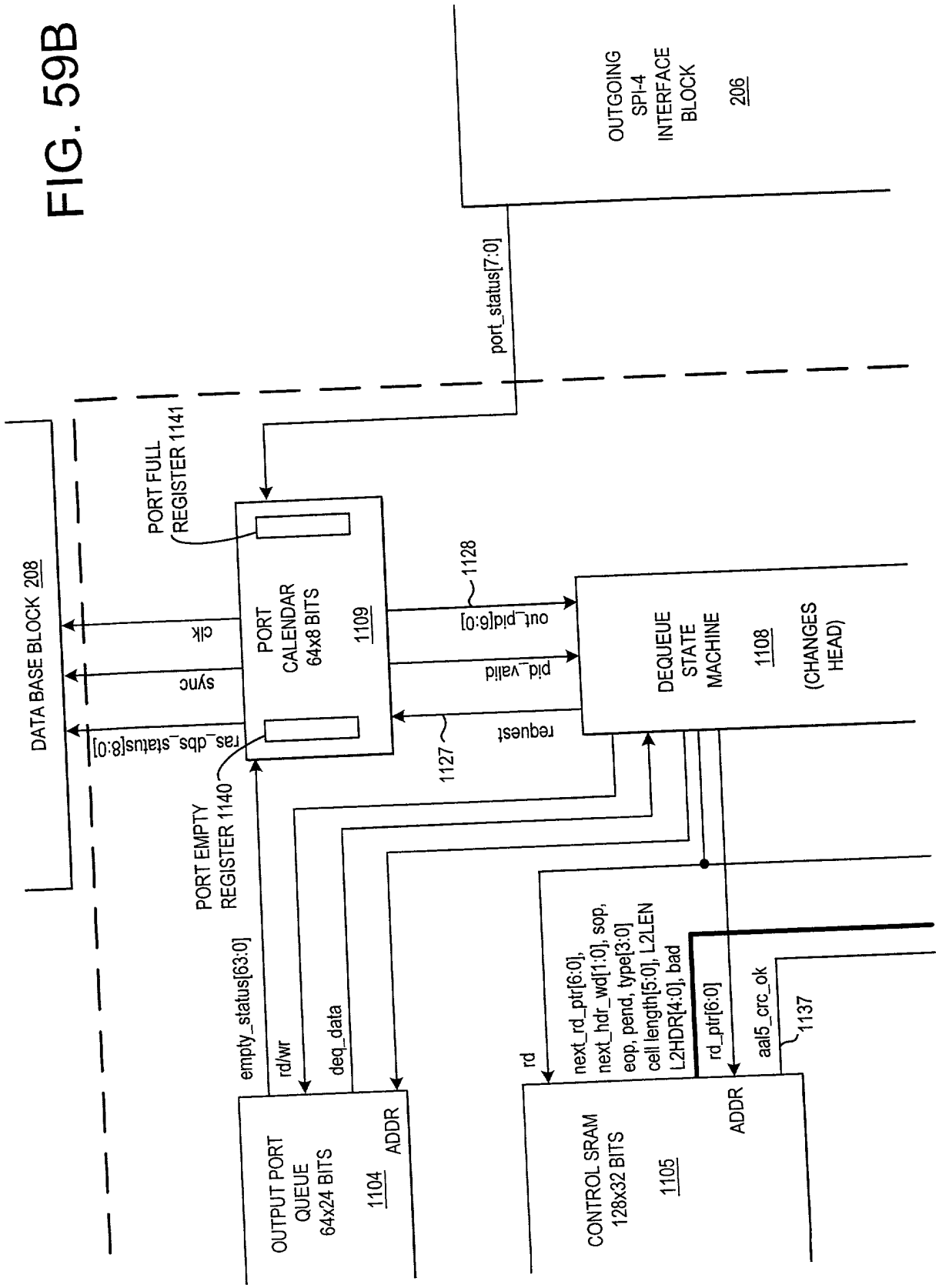


FIG. 59A

FIG. 59B


OUTGOING SPI-4 INTERFACE BLOCK 206
port_status[7:0]
DATA BASE BLOCK 208
PORT FULL REGISTER 1141
PORT CALENDAR 64x8 BITS 1109
clk
sync
ras_dbs_status[8:0]
PORT EMPTY REGISTER 1140
1128
out_pid[6:0]
pid_valid
request
1127
DEQUEUE STATE MACHINE 1108
(CHANGES HEAD)
empty_status[63:0]
rd/wr
deq_data
OUTPUT PORT QUEUE 64x24 BITS 1104
ADDR
rd
next_rd_ptr[6:0],
next_hdr_wd[1:0], sop,
eop, pend, type[3:0]
cell length[5:0], L2LEN
L2HDR[4:0], bad
rd_ptr[6:0]
aal5_crc_ok
1137
CONTROL SRAM 128x32 BITS 1105
ADDR

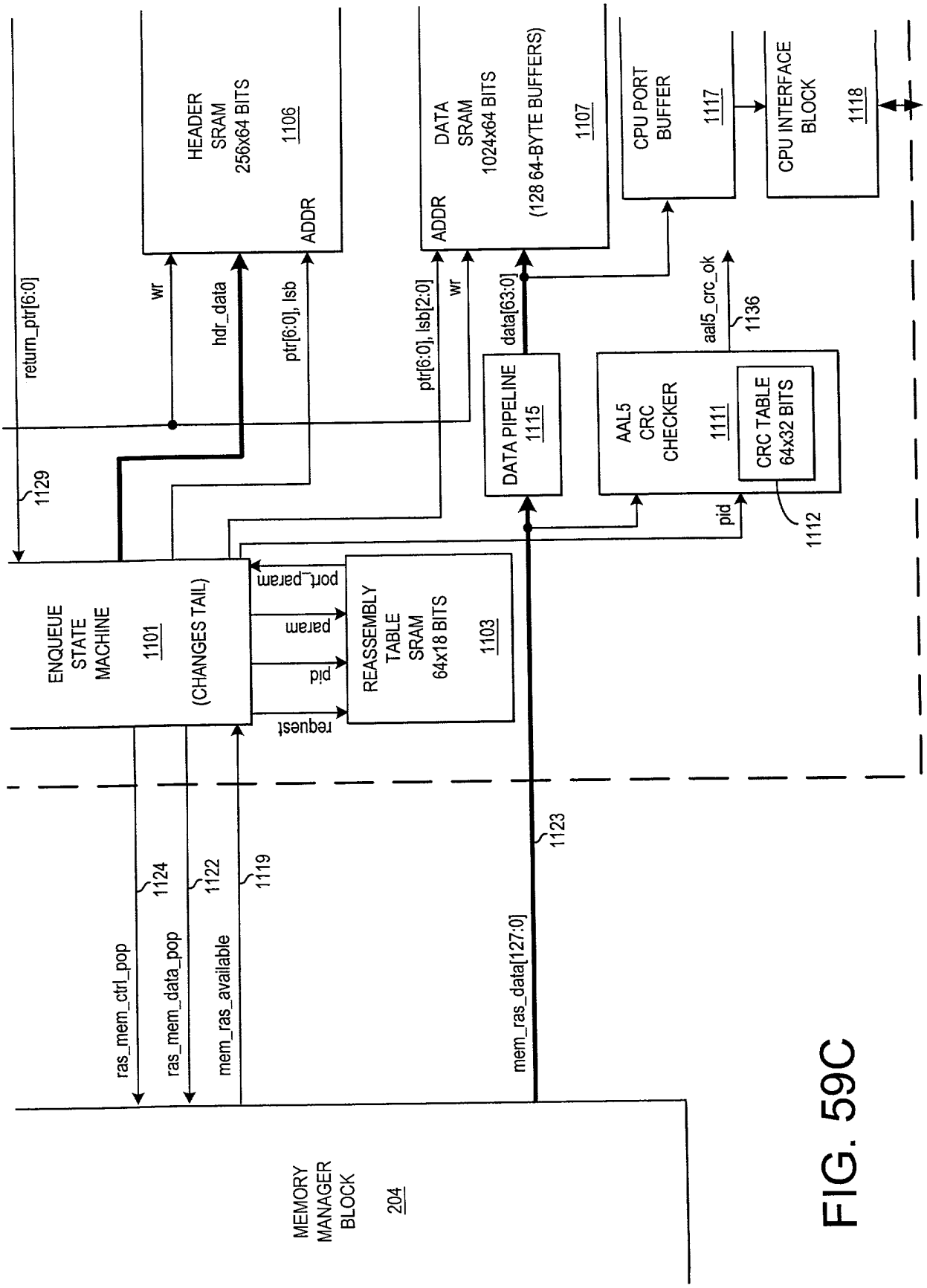

HEADER SRAM 256x64 BITS
1106
ADDR
DATA SRAM 1024x64 BITS
(128 64-BYTE BUFFERS)
1107
ADDR
CPU PORT BUFFER
1117
CPU INTERFACE BLOCK
1118
return_ptr[6:0]
wr
hdr_data
ptr[6:0], lsb
ptr[6:0], lsb[2:0]
wr
data[63:0]
aal5_crc_ok
1136
1129
DATA PIPELINE
1115
AAL5 CRC CHECKER
1111
CRC TABLE 64x32 BITS
pid
1112
ENQUEUE STATE MACHINE
1101
(CHANGES TAIL)
port_param
param
pid
request
REASSEMBLY TABLE SRAM 64x18 BITS
1103
1123
ras_mem_ctrl_pop
1124
ras_mem_data_pop
1122
mem_ras_available
1119
mem_ras_data[127:0]
MEMORY MANAGER BLOCK
204

FIG. 59C

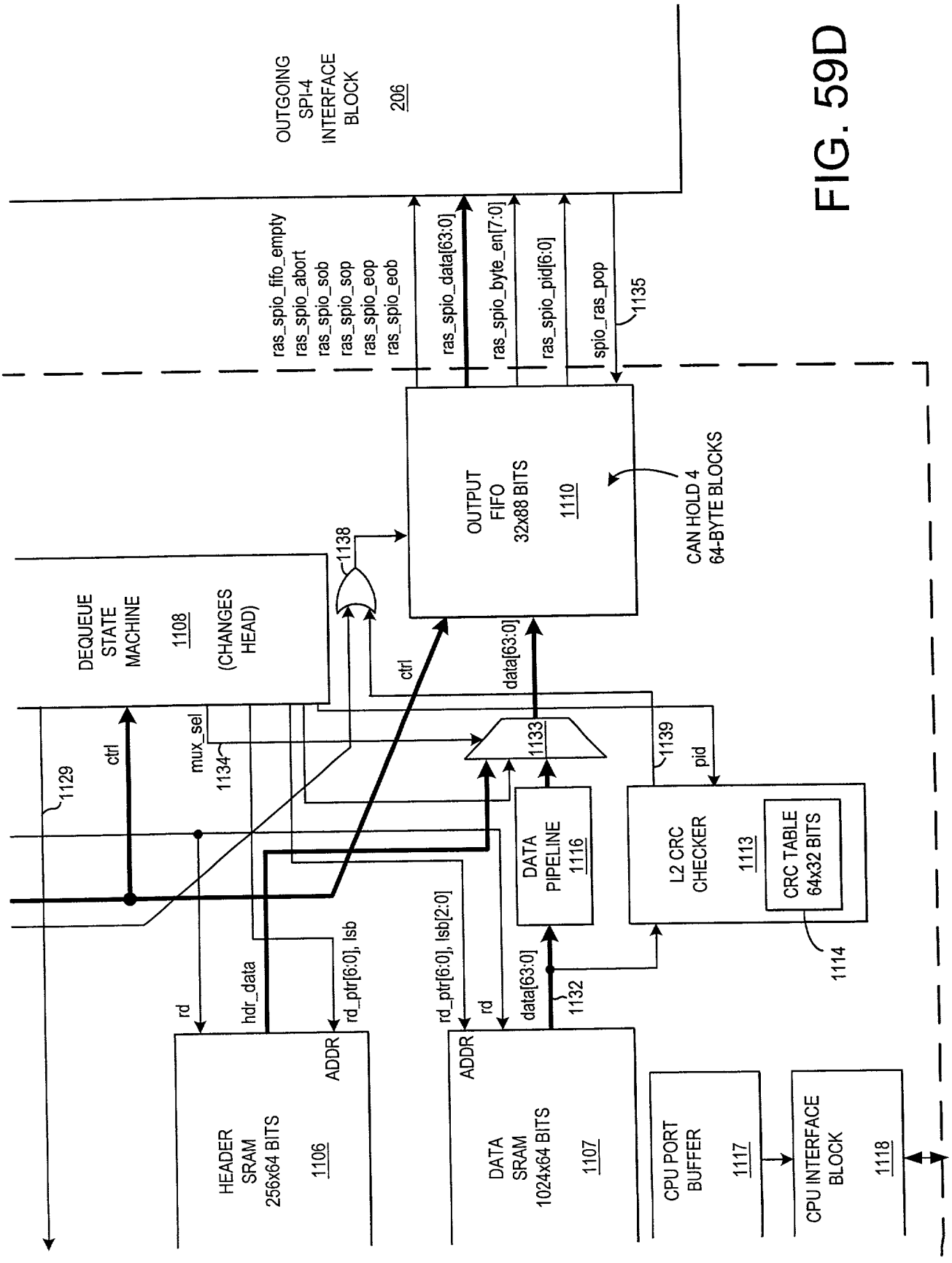
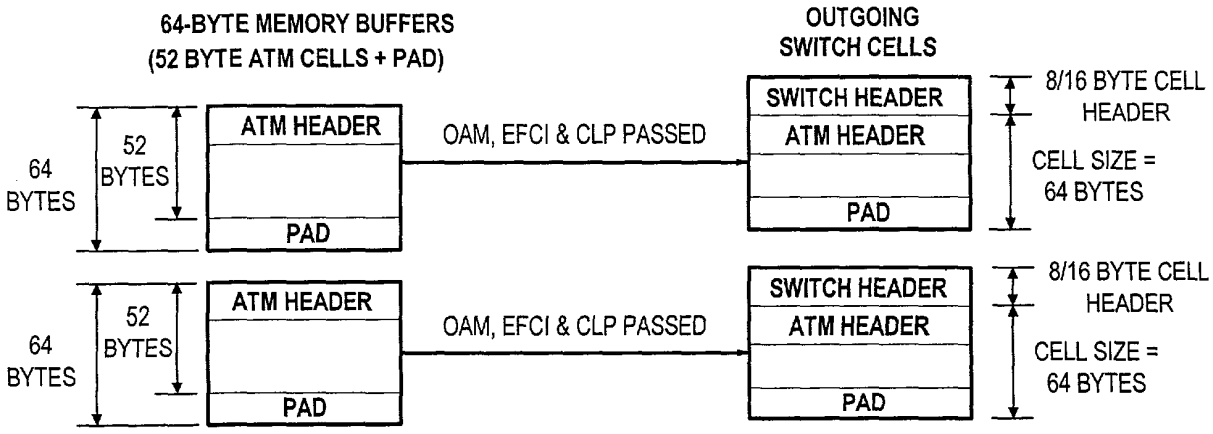
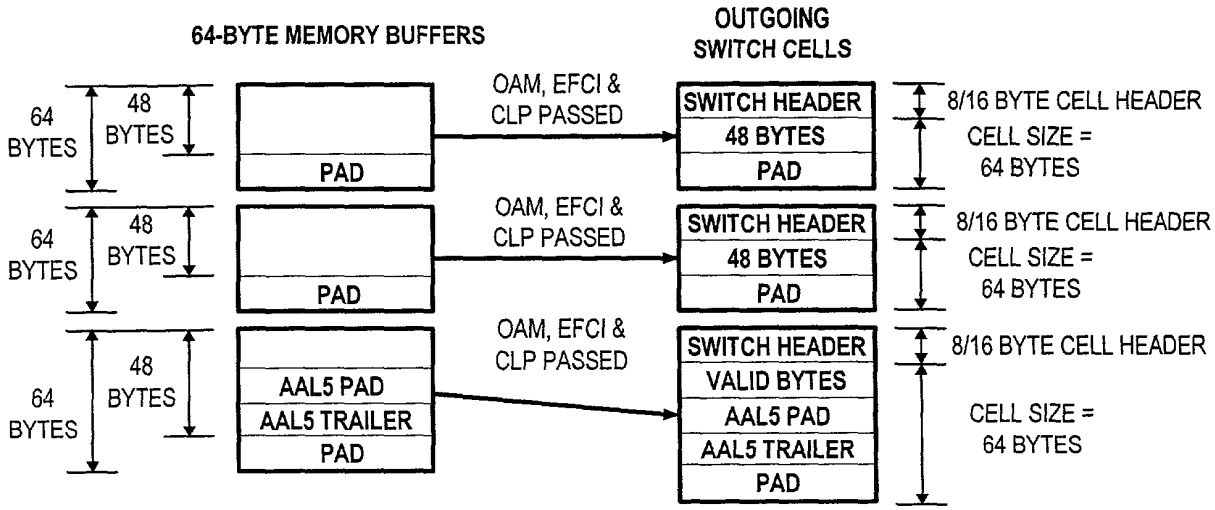

OUTGOING SPI-4 INTERFACE BLOCK
206
ras_spio_fifo_empty
ras_spio_abort
ras_spio_sob
ras_spio_sop
ras_spio_eop
ras_spio_eob
ras_spio_data[63:0]
ras_spio_byte_en[7:0]
ras_spio_pid[6:0]
spio_ras_pop
1135
OUTPUT FIFO 32x88 BITS
1110
CAN HOLD 4 64-BYTE BLOCKS
1138
DEQUEUE STATE MACHINE
1108
(CHANGES HEAD)
ctrl
data[63:0]
1133
1139
pid
1129
ctrl
mux_sel
1134
DATA PIPELINE 1116
L2 CRC CHECKER
1113
CRC TABLE 64x32 BITS
1114
rd
hdr_data
rd_ptr[6:0], lsb
rd_ptr[6:0], lsb[2:0]
rd
data[63:0]
1132
HEADER SRAM 256x64 BITS
1106
ADDR
DATA SRAM 1024x64 BITS
1107
ADDR
CPU PORT BUFFER
1117
CPU INTERFACE BLOCK
1118

FIG. 59D



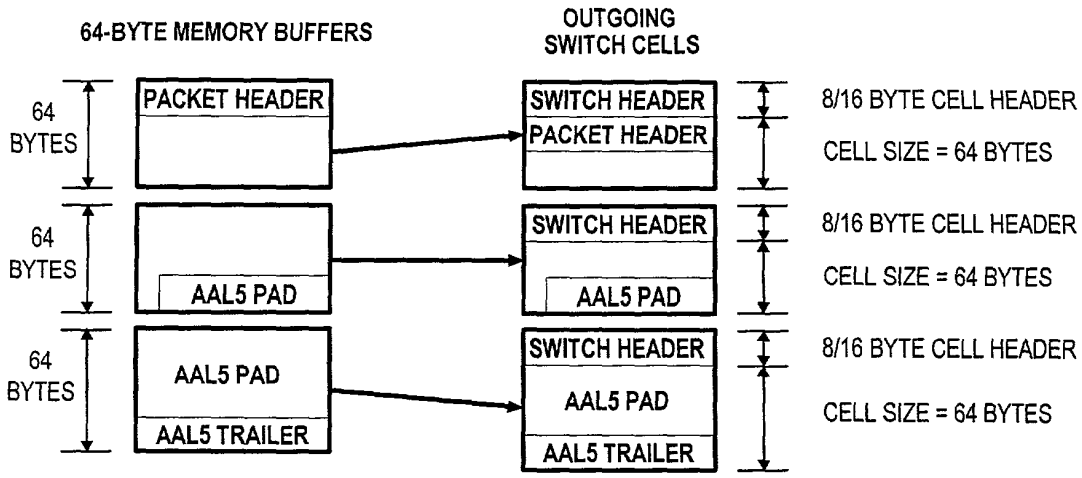
REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 0)

FIG. 60A



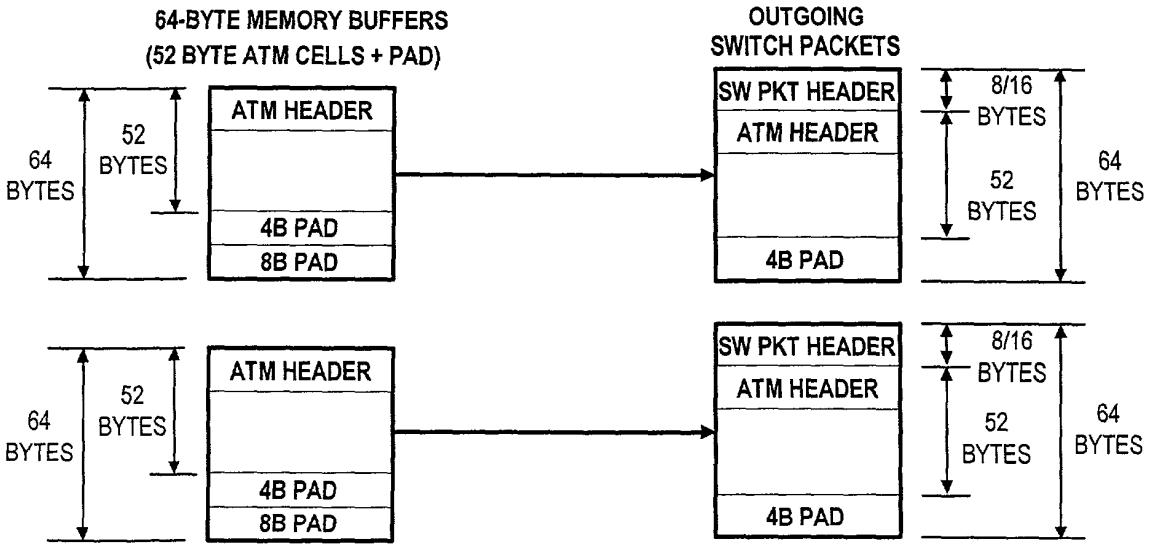
REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 1)

FIG. 60B



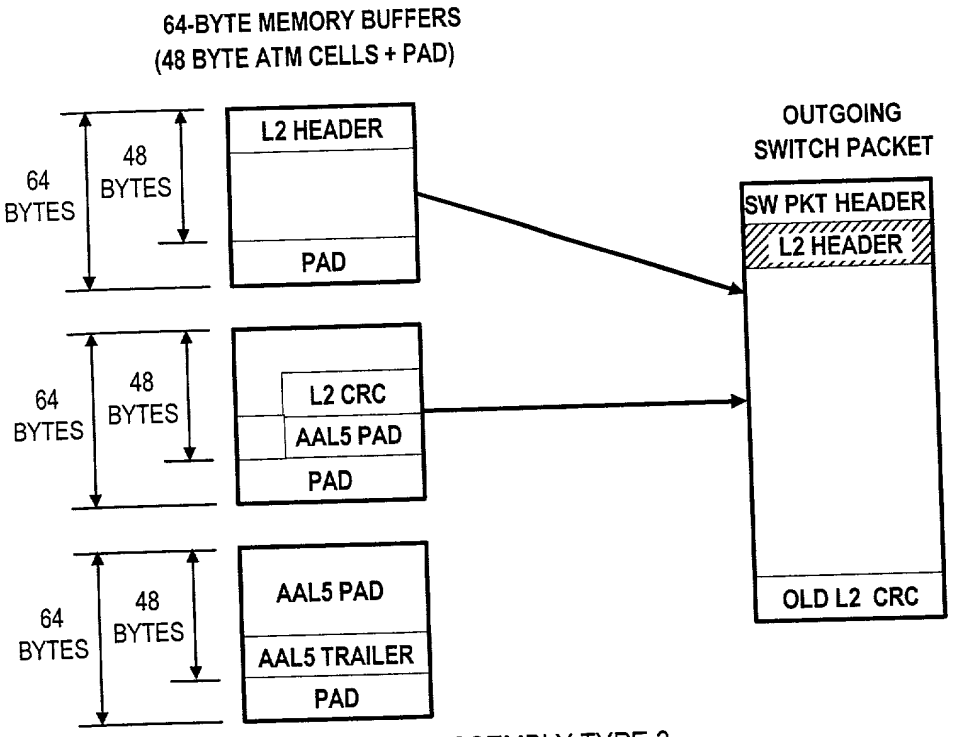
REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 3)

FIG. 60C



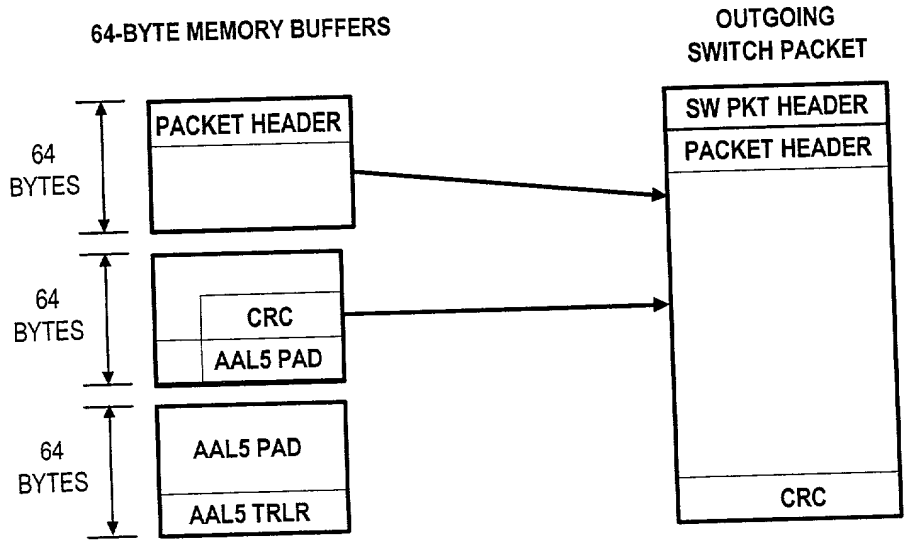
REASSEMBLY TYPE 2
(INGRESS APPLICATION TYPE 4)

FIG. 60D



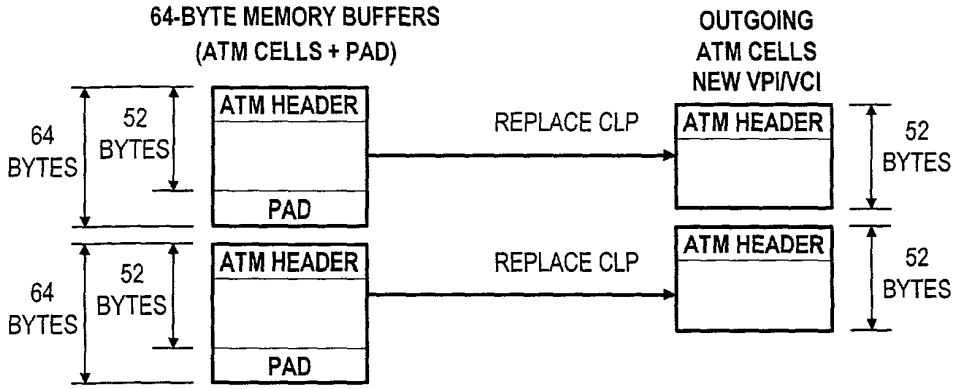
REASSEMBLY TYPE 3
(INGRESS APPLICATION TYPE 5)

FIG. 60E



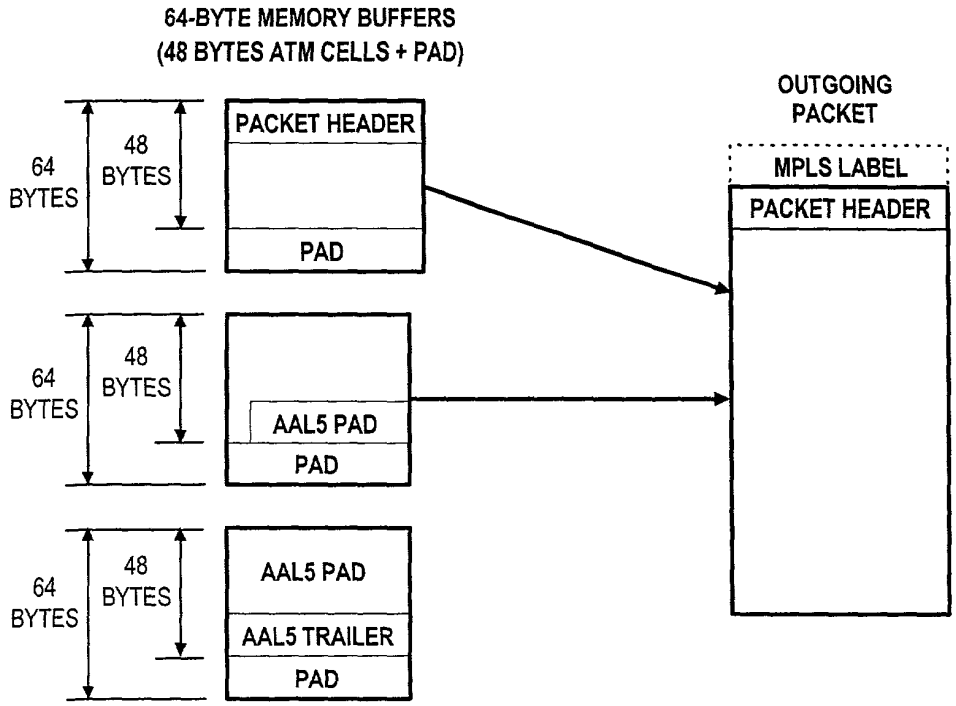
REASSEMBLY TYPE 4
(INGRESS APPLICATION TYPE 6)

FIG. 60F



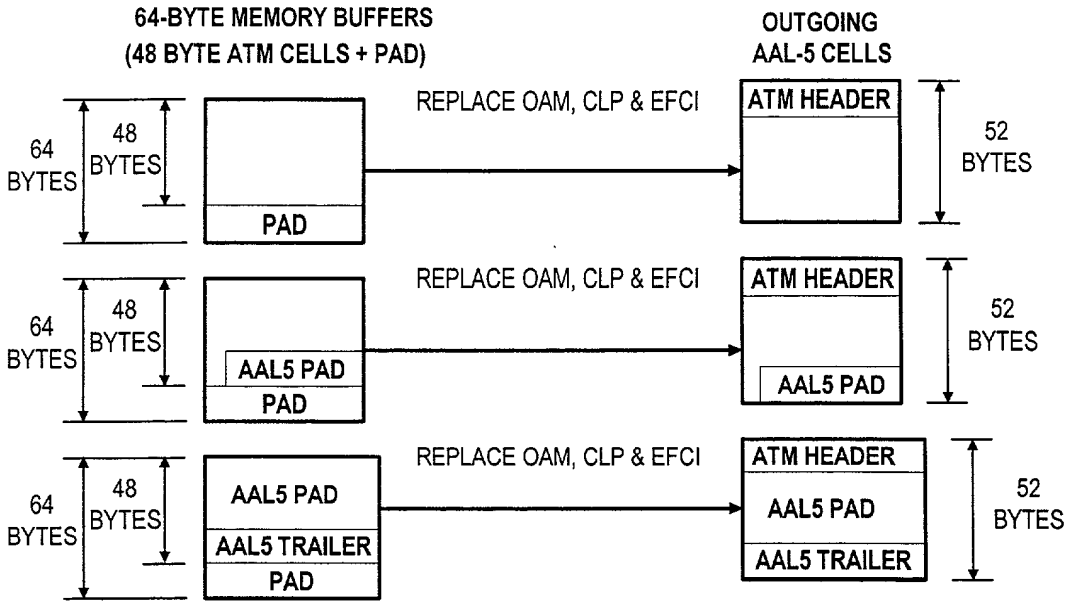
REASSEMBLY TYPE 5
(EGRESS APPLICATION TYPES 8 AND 12)

FIG. 60G



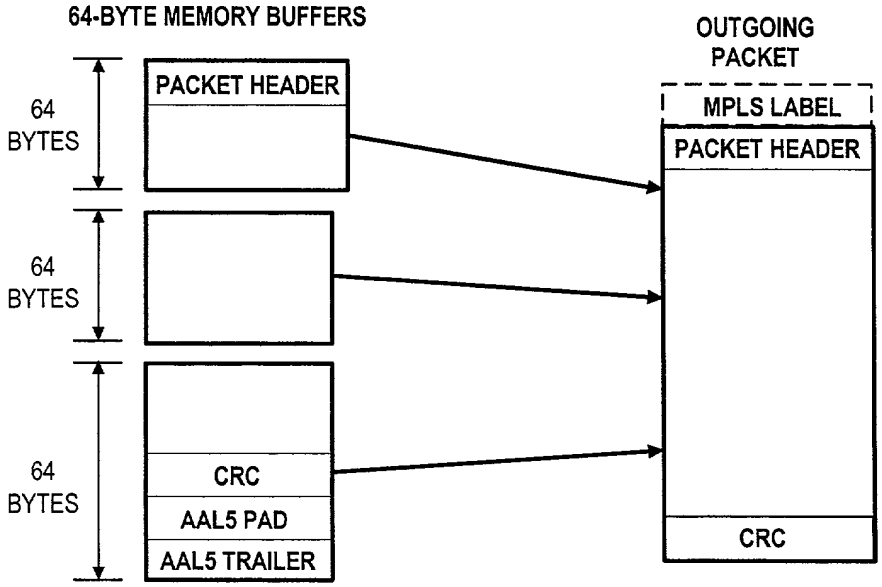
REASSEMBLY TYPE 6
(EGRESS APPLICATION TYPE 9)

FIG. 60H



REASSEMBLY TYPE 7
(INGRESS APPLICATION TYPES 10 AND 13)

FIG. 60I



REASSEMBLY TYPE 8
(INGRESS APPLICATION TYPES 11 AND 14)

FIG. 60J

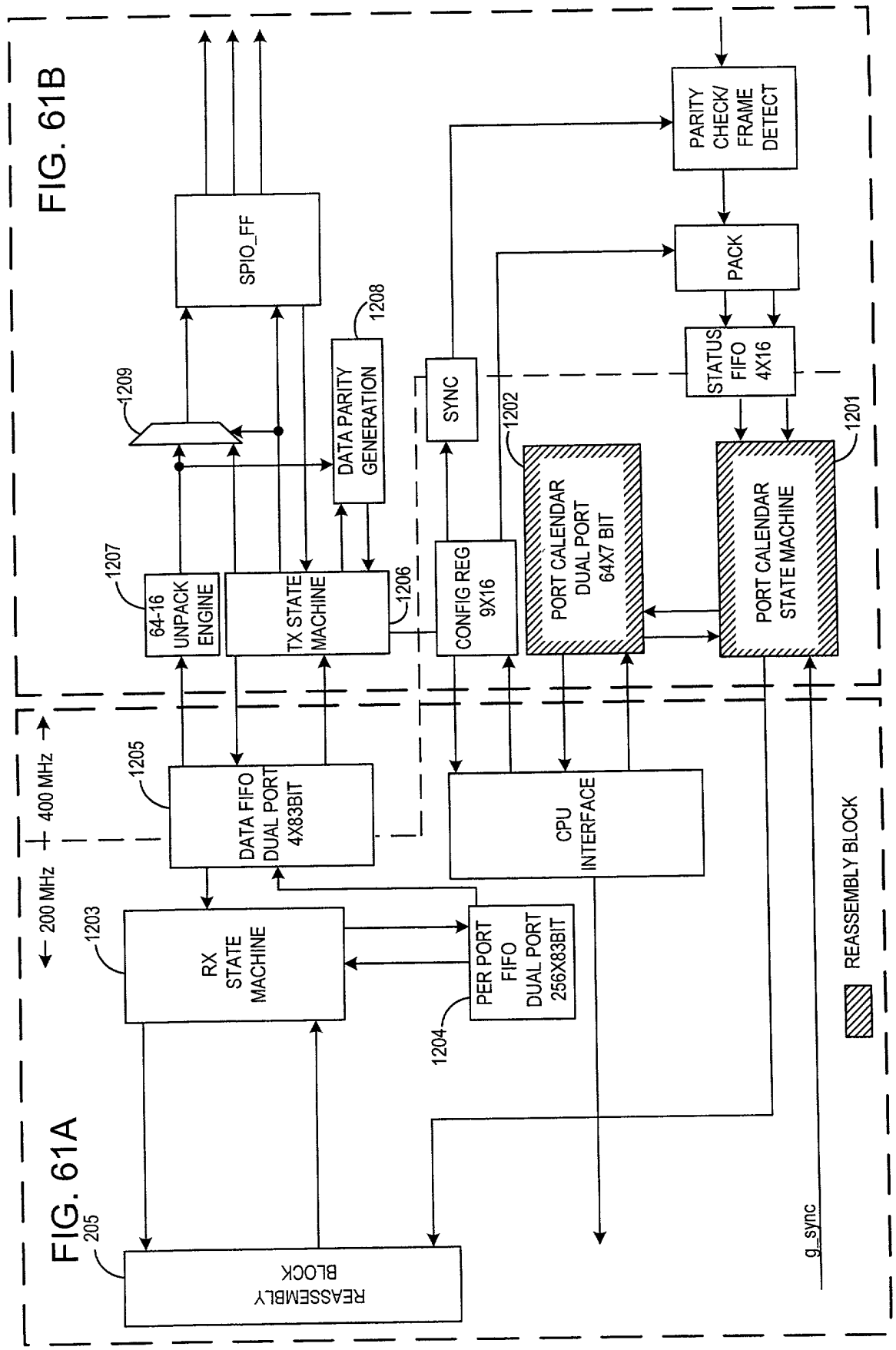


FIG. 61 OUTGOING SPI-4 INTERFACE BLOCK

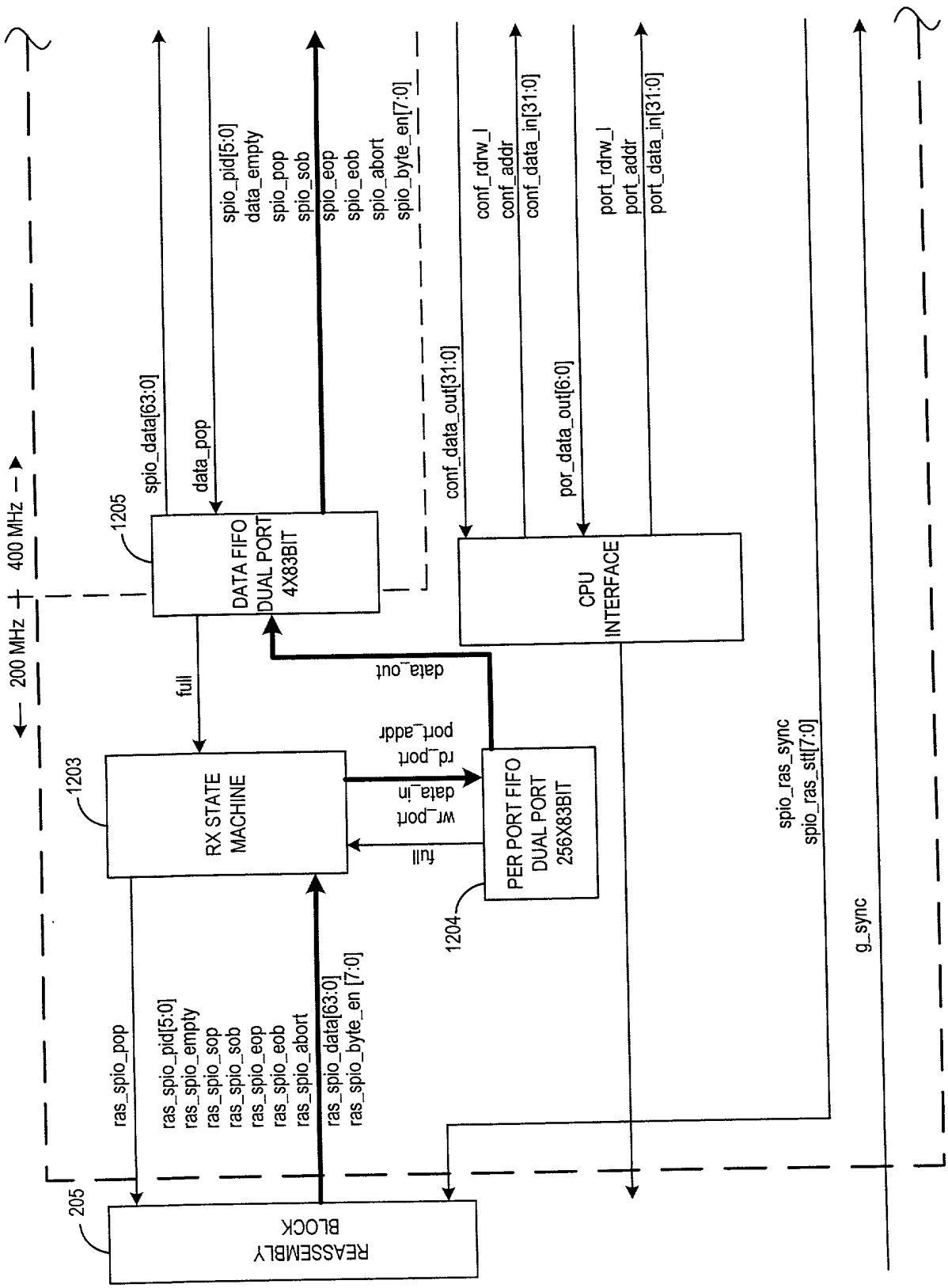


FIG. 61A OUTGOING SPI-4 INTERFACE BLOCK

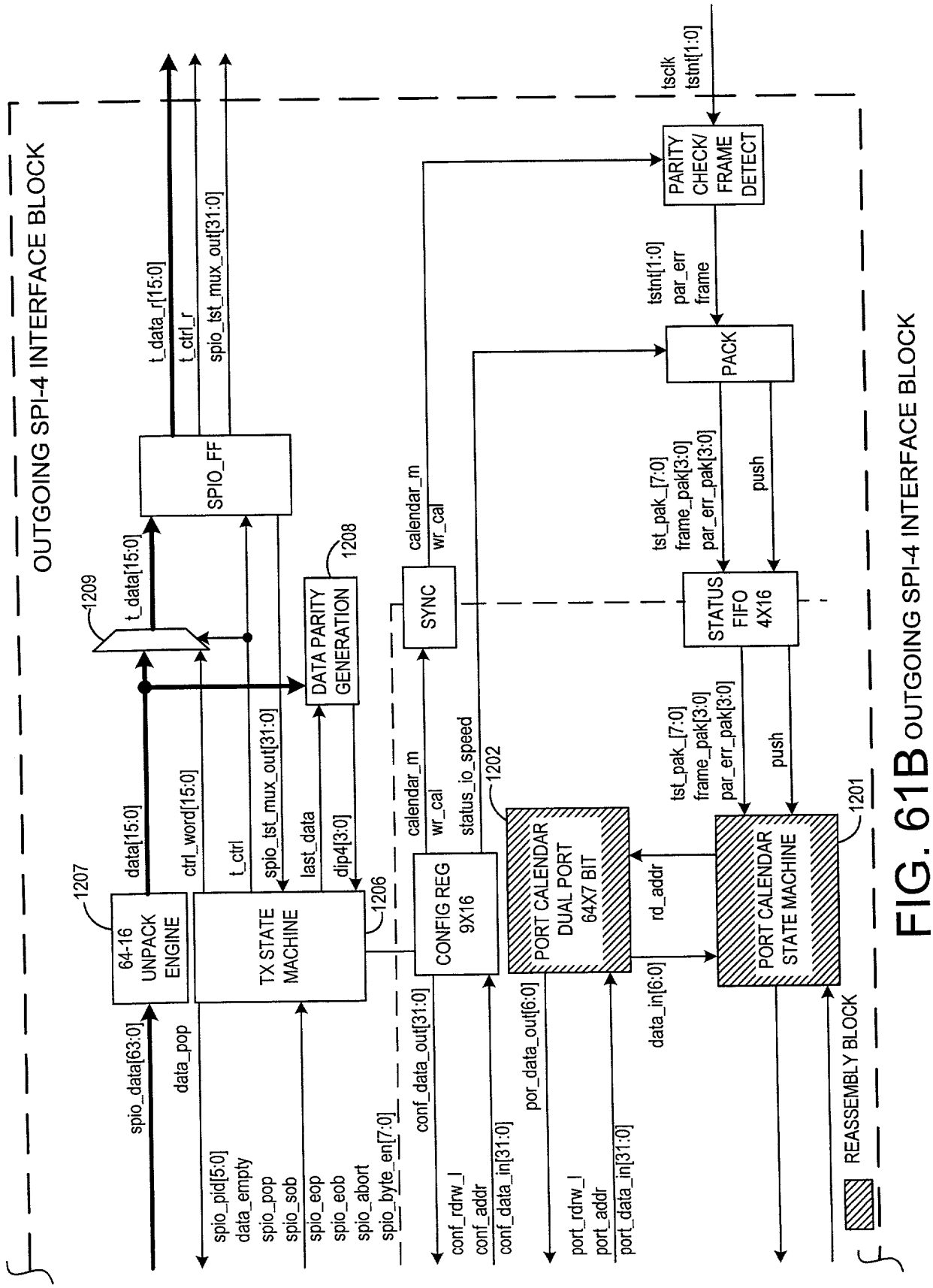


FIG. 61B OUTGOING SPI-4 INTERFACE BLOCK

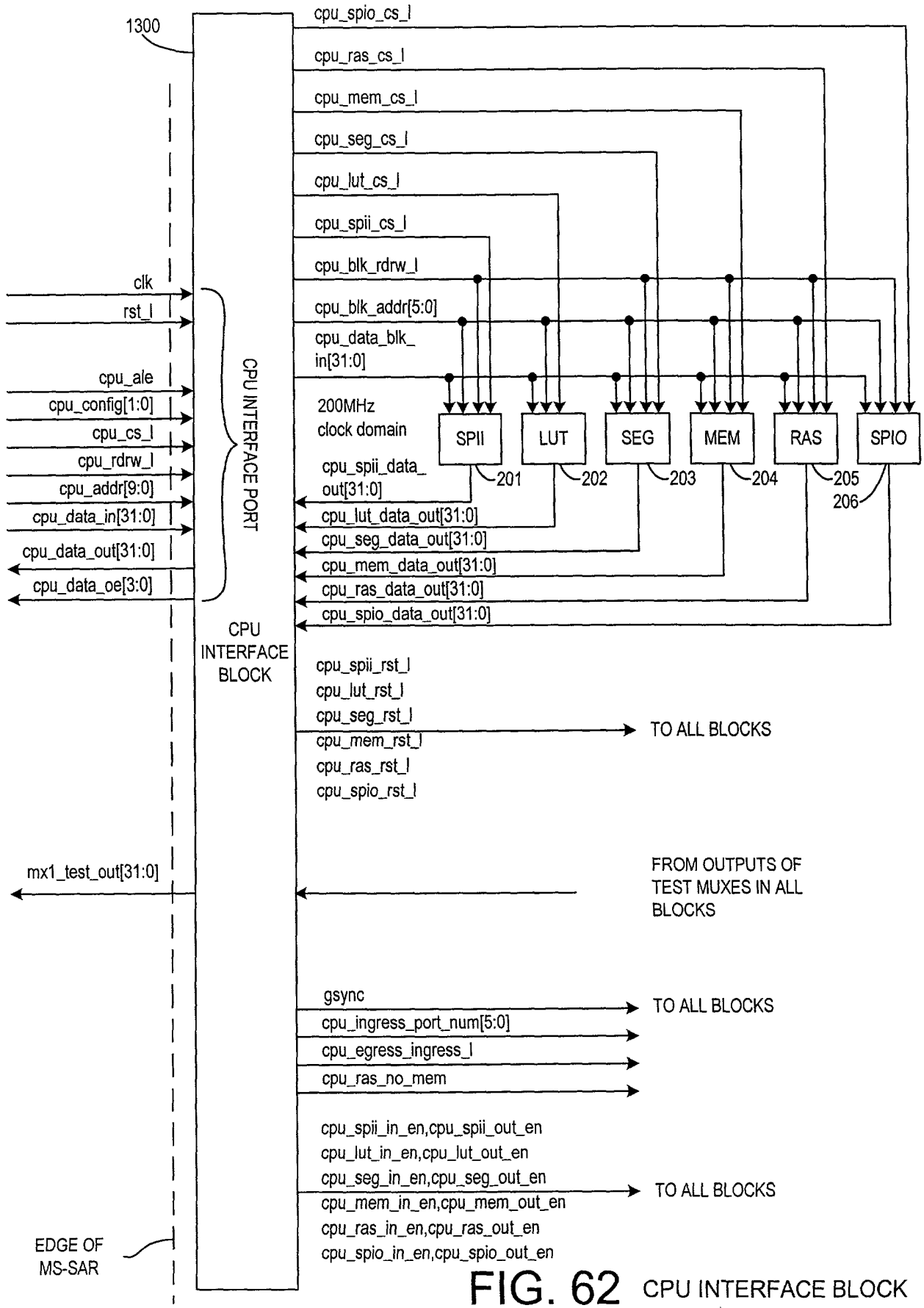


FIG. 62 CPU INTERFACE BLOCK